PXIe-1092 Specifications

2024-01-05

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PXIe-1092 Specifications. 3

PXIe-1092 Specifications

This document contains specifications for the PXIe-1092 chassis.

Caution Specifications are subject to change without notice.

Electrical

The following section provides information about the PXIe-1092 AC input and DC output.

AC Input

Input rating[1]	100 to 240 VAC, 50/60 Hz, 15 to 7.5 A 100 to 120 VAC, 440 Hz, 15 A
Operating voltage range[2][2]	90 to 264 VAC
Nominal input frequency	50 Hz/60 Hz/400 Hz [3]
Operating frequency range[2]	47 to 440 Hz
Efficiency	85% typical
Over-current protection	Internal fuse in line
Main power disconnect	The AC power cable provides main power disconnect. Do not position the equipment so that it is difficult to disconnect the power cord. The front-panel power switch causes the

[1] Care must be taken to not exceed the current rating of the branch circuit providing power to the chassis.
[2] The operating range is guaranteed by design.
[3] 400 Hz operation only supported from 100 to 120 VAC.

	internal chassis power supply to provide DC power to the PXI Express backplane. With the Timing and Synchronization upgrade, you also can use the rear-panel 15-pin connector and inhibit mode switch to control the internal chassis power supply.

Caution Disconnect power cord to completely remove power.

DC Output

DC output characteristics of the PXIe-1092.

Voltage Rail	Maximum Current	Load Regulation	Maximum Ripple and Noise (20 MHz BW)
+5V_AUX	3 A	±5%	50 mVpp
+12 V	74 A	±5%	100 mVpp
+5 V	26.5 A	±5%	50 mVpp
+3.3 V	36 A	±5%	50 mVpp
-12 V	1.75 A	±5%	50 mVpp

Maximum total available power for the PXIe-1092 is 988 W.

Table 1. Backplane Slot Current Capacity

Slot	+5 V	V (I/O)	+3.3 V	+12 V	-12 V	5 V_{AUX}
System Controller Slot	15 A	-	15 A	30 A	-	3 A
System Timing Slot	-	-	9 A	6 A	-	1 A
Hybrid Peripheral Slot with PXI-5 Peripheral	-	-	9 A	6 A	-	1 A

Slot	+5 V	V (I/O)	+3.3 V	+12 V	-12 V	5 V_{AUX}
Hybrid Peripheral Slot with PXI-1 Peripheral	6 A	5 A	6 A	1 A	1 A	-
Expansion Slot	-	-	9 A	6 A	-	1 A

Note Total System Controller Slot current should not exceed 45 A.

Note PCI V(I/O) pins in Hybrid Peripheral Slots are connected to +5 V.

Note The maximum power dissipated in a peripheral slot should not exceed 82 W.

Over-current protection	All outputs protected from short circuit and overload with automatic recovery
Over-voltage protection	+12 V, +5 V, and +3.3 V clamped at 20 to 30% above nominal output voltage
Power supply MTTR	Replacement in under 1 minute

Chassis Cooling

Module cooling	Forced air circulation (positive pressurization) through two 210 CFM fans
Module slot airflow direction	Bottom of module to top of module
Module intake	Rear of chassis

Module exhaust	Top of chassis
Slot cooling capacity	82 W
Secondary cooling	Forced air circulation (positive pressurization) through one 70 CFM fan
Side intake	Right side of chassis
Side exhaust	Left side of chassis
Power supply cooling	Forced air circulation through two integrated fans
Power supply intake	Rear of chassis
Power supply exhaust	Top of chassis
Timing and Synchronization upgrade intake	Right side of chassis
Timing and Synchronization upgrade exhaust	Top of chassis
Minimum chassis cooling clearances	
Above	44.45 mm (1.75 in.)
Rear	101.60 mm (4.00 in.)
Sides	44.45 mm (1.75 in.)

Environmental

Maximum altitude	4,600 m (15,000 ft.), 570 mbar (at 25 °C ambient, high fan mode)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	
When all peripheral modules require ≤58 W cooling capacity per slot	0 °C to 55 °C (IEC 60068-2-1 and IEC 60068-2-2.)[4] Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.
When any peripheral module requires >58 W cooling capacity per slot	0 °C to 40 °C (IEC 60068-2-1 and IEC 60068-2-2.)[4] Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 4 high temperature limit.
Relative humidity range	10% to 90%, noncondensing (IEC 60068-2-78.)[4]

Storage Environment

Ambient temperature range	–40 °C to 71 °C (IEC-60068-2-1 and IEC-60068-2-2.)[5] Meets MIL-PRF-28800F Class 3 limits.
Relative humidity range	5% to 95%, noncondensing (IEC-60068-2-78.)[5]

[4] This product meets the requirements of the environmental standards for electrical equipment for measurement, control, and laboratory use.

[5] This product meets the requirements of the environmental standards for electrical equipment for measurement, control, and laboratory use.

Shock and Vibration

Operational shock	30 g peak, half-sine, 11 ms pulse (IEC-60068-2-27.)[3] Meets MIL-PRF-28800F Class 2 limits.
Operational random vibration	5 to 500 Hz, 0.3 g_{rms}
Non-operating vibration	5 to 500 Hz, 2.4 g_{rms} (IEC 60068-2-64.)[3] Non-operating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.

Acoustic Emissions

Sound Pressure Level (at Operator Position)

(Tested in accordance with ISO 7779. Meets MIL-PRF-28800F requirements.)

38 W Profile	
Auto fan (up to 30 °C ambient)	35.9 dBA
High fan	55.7 dBA

58 W/82 W Profile	
Auto fan (up to 30 °C ambient)	50.7 dBA
High fan	63.4 dBA

Sound Power Level

38 W Profile

Auto fan (up to 30 °C ambient)	47.5 dBA
High fan	66.2 dBA

58 W/82 W Profile	
Auto fan (up to 30 °C ambient)	61.6 dBA
High fan	74.5 dBA

Note The protection provided by the PXIe-1092 can be impaired if it is used in a manner not described in this document.

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility Standards

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity

- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

Note For EMC declarations and certifications, and additional information, refer to the Product Certifications and Declarations section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2011/65/EU; Restriction of Hazardous Substances (RoHS)
- 2014/53/EU; Radio Equipment Directive (RED)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI

products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Backplane

Size	3U-sized; one system slot (with three system expansion slots), eight peripheral slots, and one peripheral expansion slot. Compliant with IEEE 1101.10 mechanical packaging. PXI Express Specification compliant. Accepts both PXI Express and CompactPCI (PICMG 2.0 R 3.0) 3U modules.
Backplane bare-board material	UL 94 V-0 Recognized
Backplane connectors	Conforms to IEC 917 and IEC 1076-4-101, UL 94 V-0 rated

System Synchronization Clocks

10 MHz System Reference Clock: PXI_CLK10

Maximum slot-to-slot skew	250 ps
Accuracy	±25 ppm max (guaranteed over the operating temperature range)
Accuracy with OCXO (Timing and Synchronization option)	±80 ppb max within 1 year of calibration adjustment within 0 °C to 55 °C operating temperature range (after 24 hours of operation); ±50 ppb/year long-term stability (after 72 hours of operation)
Maximum jitter	5 ps RMS phase-jitter (10 Hz–1 MHz range)

Duty-factor	45% to 55%
Unloaded signal swing	3.3 V ±0.3 V

Note For other specifications, refer to the **PXI-1 Hardware Specification**.

100 MHz System Reference Clock: PXIe_CLK100 and PXIe_SYNC100

Maximum slot-to-slot skew	100 ps
Accuracy	±25 ppm max (guaranteed over the operating temperature range)
Accuracy with OCXO (Timing and Synchronization option)	±80 ppb max within 1 year of calibration adjustment within 0 °C to 55 °C operating temperature range (after 24 hours of operation); ±50 ppb/year long-term stability (after 72 hours of operation)
Maximum jitter	3 ps RMS phase-jitter (10 Hz to 12 kHz range), 2 ps RMS phase-jitter (12 kHz to 20 MHz range)
Duty-factor for PXIe_CLK100	45% to 55%
Absolute differential voltage (When terminated with a 50 Ω load to 1.30 V or Thévenin equivalent)	400 to 1000 mV

Note For other specifications, refer to the **PXI-5 PXI Express Hardware Specification**

External 10 MHz Reference Out (Timing and Synchronization Option, Rear Panel SMA)

Accuracy	±80 ppb max within 1 year of calibration adjustment within 0 °C to 55 °C operating temperature range (after 24 hours of operation); ±50 ppb/year long-term stability (after 72 hours of operation)
Maximum jitter	5 ps RMS phase-jitter (10 Hz–1 MHz range)
Output amplitude	1 Vpp ±20% square-wave into 50Ω, 2 Vpp unloaded
Output impedance	50Ω ±5Ω

External Clock Source

Frequency	10 MHz ±25 ppm
Input amplitude	
External 10 MHz Reference IN (Timing and Synchronization option, rear panel SMA)	100 mVpp to 5 Vpp square-wave or sine-wave
System timing slot PXI_CLK10_IN	5 V or 3.3 V TTL signal
Maximum jitter introduced by backplane	1 ps RMS phase-jitter (10 Hz to 1 MHz range)
Rear panel SMA input impedance (Timing and Synchronization option)	50 Ω ±5 Ω

PXI Star Trigger

Maximum slot-to-slot skew	250 ps
Backplane characteristic impedance	65 Ω ±10%

For other specifications, refer to the **PXI-1 Hardware Specification**.

PXI Differential Star Triggers

(PXIe-DSTARA, PXIe-DSTARB, PXIe-DSTARC)

Maximum slot-to-slot skew	150 ps
Maximum differential skew	25 ps
Backplane differential impedance	100 Ω ±10%

For other specifications, the PXIe-1092 complies with the **PXI-5 PXI Express Hardware Specification**.

Remote Inhibit and Chassis Monitoring Connector (Timing and Synchronization Option)

Inhibit input signal	
Input voltage range	-0.5 V min to 5.5 V max
V_{IH}	2.0 V
V_{IL}	0.8 V
Input impedance	High-Z (>10 kΩ typical)

Note Internal 10 kΩ pull-up to an internal +3.3V_AUX rail.

Fault output signal	
Output voltage range	0 V to 3.3 V typical
V_{OH}	2.4 V min ($\|I_{OH}\|$ < 8 mA)
V_{OL}	0.4 V max ($\|I_{OL}\|$ < 8 mA)
Output impedance	65 Ω typical
PFI lines	
Input voltage range	-0.5 V min to 4.6 V max
V_{IH}	2.0 V
V_{IL}	0.8 V
Input impedance	High-Z (>10 kΩ typical)
Output voltage range	0 V to 3.3 V typical
V_{OH}	2.4 V min ($\|I_{OH}\|$ < 8 mA)
V_{OL}	0.4 V max ($\|I_{OL}\|$ < 8 mA)
Output impedance	65 Ω typical

Mechanical

Standard chassis dimensions

Height	177.1 mm (6.97 in.)
Width	303.3 mm (11.94 in.)
Depth	463.6 mm (18.25 in.)

Weight	12.3 kg (27.1 lb)

Chassis materials	Sheet Aluminum (5052-H32, 5754-H22), Extruded Aluminum (6063-T5, 6060-T6), Plate Aluminum (6063-T5, 6061-T6), Cold Rolled Steel, Cold Rolled Stainless Steel, Sheet Copper (C110), Santoprene, Urethane Foam, PC-ABS, Nylon, Polycarbonate, Polyethylene, Polyamide (FR-106)
Finish	Conductive Clear Iridite on Aluminum, Electroplated Nickel on Cold Rolled Steel, Electroplated Zinc on Cold Rolled Steel, Electroplated Nickel on Copper

The following figures show the PXIe-1092 chassis dimensions. The holes shown are for the installation of the optional rack mount kits.

Figure 1. PXIe-1092 Chassis Dimensions (front)

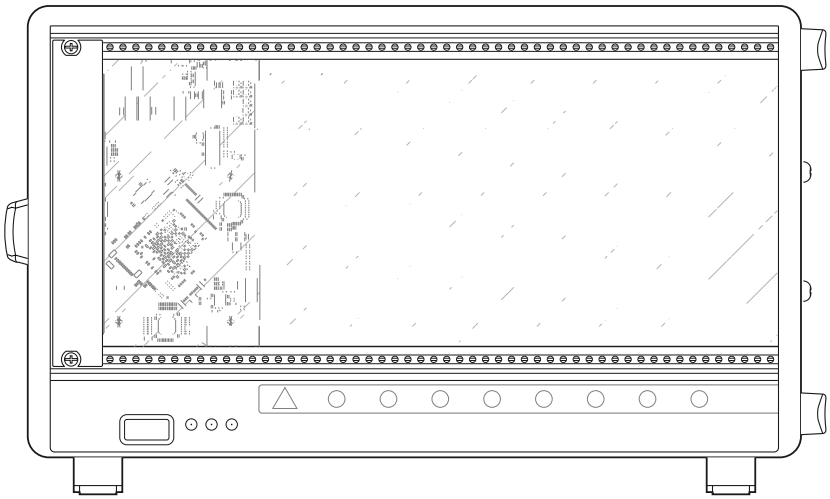


Figure 2. PXIe-1092 Chassis Dimensions (side)

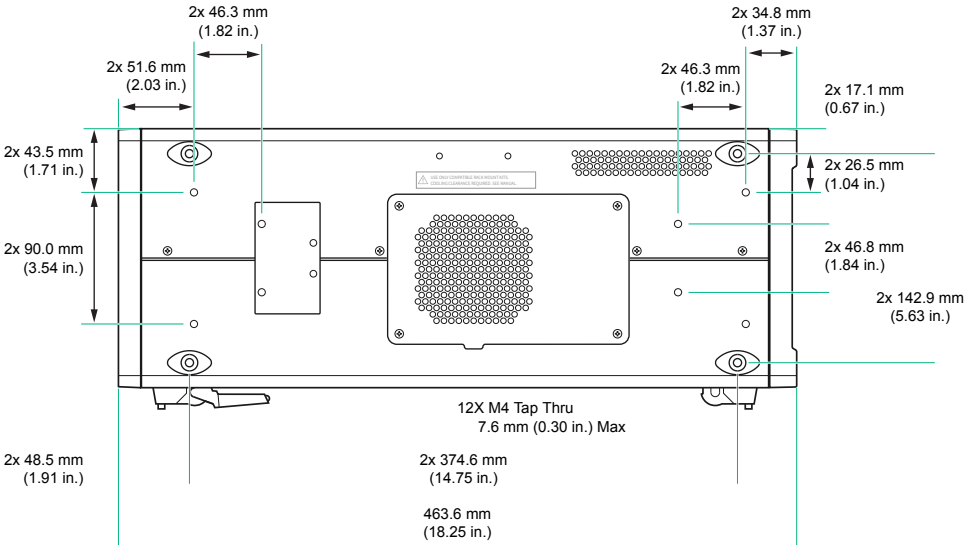
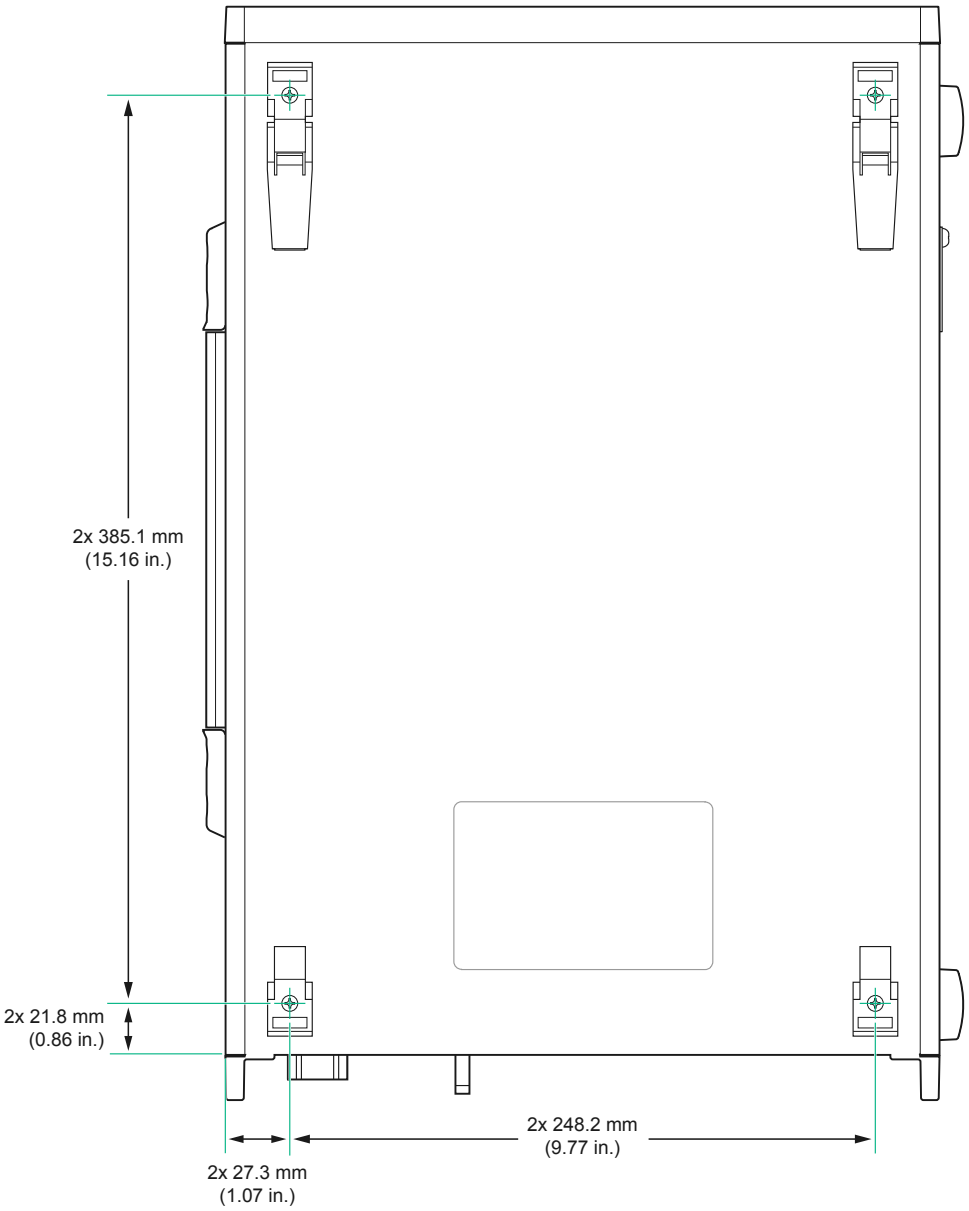


Figure 3. PXIe-1092 Chassis Dimensions (bottom)



PXIe-6363 Specifications

2024-01-05

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PXIe-6363 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are **Typical** unless otherwise noted.

Conditions

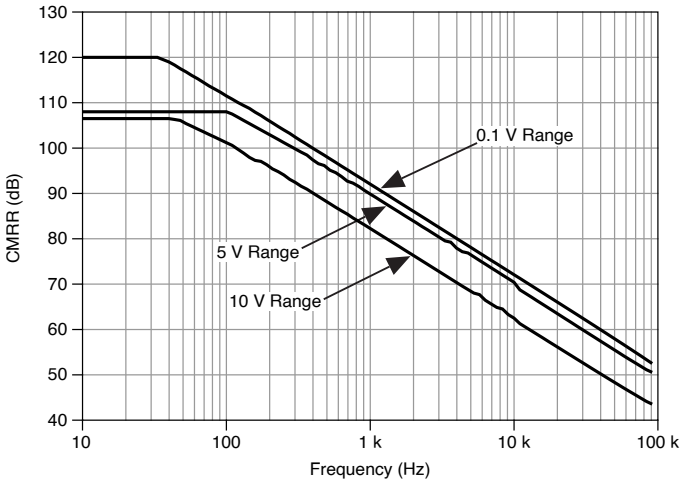
Specifications are valid at 25 °C unless otherwise noted.

Analog Input

Number of channels	32 single-ended or 16 differential
ADC resolution	16 bits
DNL	No missing codes guaranteed
INL	Refer to **AI Absolute Accuracy**.
Sample rate	

Single channel maximum	2.00 MSample/s
Multichannel maximum (aggregate)	1.00 MSample/s
Minimum	No minimum
Timing resolution	10 ns
Timing accuracy	50 ppm of sample rate
Input coupling	DC
Input range	±0.1 V, ±0.2 V, ±0.5 V, ±1 V, ±2 V, ±5 V, ±10 V
Maximum working voltage for analog inputs (signal + common mode)	±11 V of AI GND
CMRR (DC to 60 Hz)	100 dB

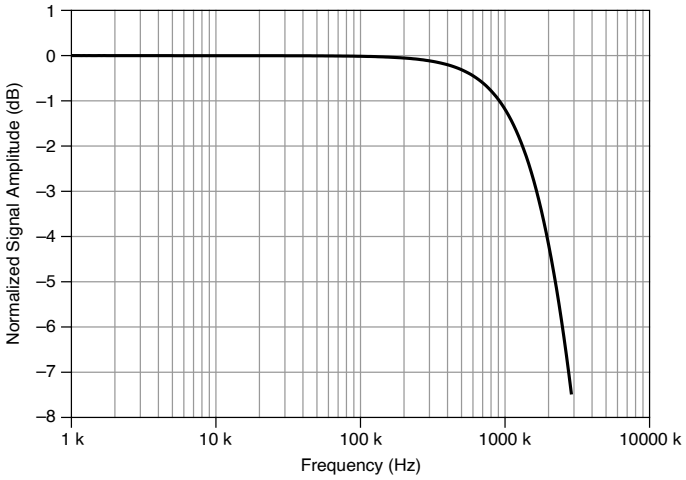
Figure 1. AI <0..31> CMRR



Input impedance
Device on

AI+ to AI GND	>10 GΩ in parallel with 100 pF
AI- to AI GND	>10 GΩ in parallel with 100 pF
Device off	
AI+ to AI GND	820 Ω
AI- to AI GND	820 Ω
Input bias current	±100 pA
Crosstalk (at 100 kHz)	
Adjacent channels	-75 dB
Non-adjacent channels	-95 dB
Small signal bandwidth (-3 dB)	1.7 MHz

Figure 2. AI <0..31> Small Signal Bandwidth



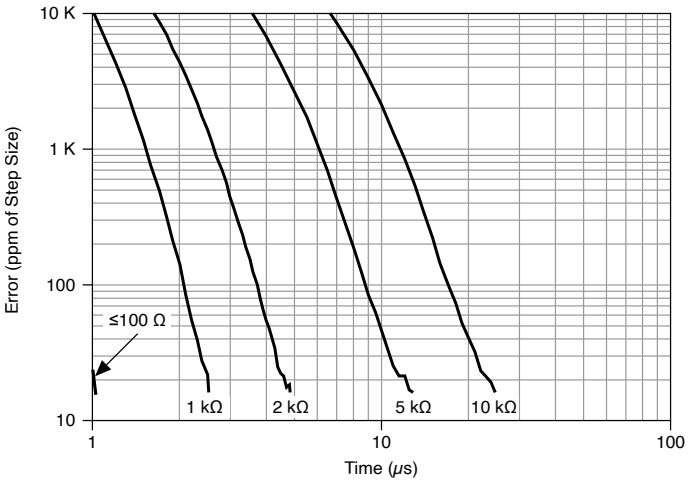
Input FIFO size	2,047 samples
Scan list memory	4,095 entries

Data transfers	DMA (scatter-gather), programmed I/O
Overvoltage protection for all analog input and sense channels	
Device on	±25 V for up to two AI pins
Device off	±15 V for up to two AI pins
Input current during overvoltage condition	±20 mA max/AI pin

Table 1. Settling Time for Multichannel Measurements

Range	±60 ppm of Step (±4 LSB for Full-Scale Step)	±15 ppm of Step (±1 LSB for Full-Scale Step)
± 10 V, ±5 V, ±2 V, ±1 V	1 µs	1.5 µs
±0.5 V	1.5 µs	2 µs
±0.2 V, ±0.1 V	2 µs	8 µs

Figure 3. Settling Error versus Time for Different Source Impedances



Analog Triggers

Number of triggers	1
Source	AI <0..31>, APFI <0,1>

Functions	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Source level	
AI <0..31>	±Full scale
APFI <0,1>	±10 V
Resolution	16 bits
Modes	Analog edge triggering, analog edge triggering with hysteresis, analog window triggering
Bandwidth (-3 dB)	
AI <0..31>	3.4 MHz
APFI <0,1>	3.9 MHz
Accuracy	±1% of range
APFI <0,1> characteristics	
Input impedance	10 kΩ
Coupling	DC
Protection	
Power on	±30 V
Power off	±15 V

AI Absolute Accuracy (Warranted)

Table 2. AI Absolute Accuracy

Nominal Range Positive Full Scale (V)	Nominal Range Negative Full Scale (V)	Residual Gain Error (ppm of Reading)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	Random Noise, σ (µVrms)	Absolute Accuracy at Full Scale (µV)
10	-10	48	13	21	315	1,660
5	-5	55	13	21	157	870
2	-2	55	13	24	64	350
1	-1	65	17	27	38	190
0.5	-0.5	68	17	34	27	100
0.2	-0.2	95	27	55	21	53
0.1	-0.1	108	45	90	17	33

Note **Absolute Accuracy at Full Scale** is determined using the following assumptions:

- TempChangeFromLastExternalCal = 10 °C
- TempChangeFromLastInternalCal = 1 °C
- NumberOfReadings = 10,000
- CoverageFactor = 3 σ

Note Accuracies listed are valid for up to two years from the device external calibration.

Gain tempco	13 ppm/°C
Reference tempco	1 ppm/°C
INL error	60 ppm of range

AI Absolute Accuracy Equation

AbsoluteAccuracy = Reading · (GainError) + Range · (OffsetError) + NoiseUncertainty

- GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)
- OffsetError = ResidualOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INLError
- NoiseUncertainty = $\frac{\text{Random Noise} \quad 3}{\sqrt{10,000}}$ for a coverage factor of 3 σ and averaging 10,000 points.

AI Absolute Accuracy Example

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

- GainError: 48 ppm + 13 ppm · 1 + 1 ppm · 10 = 71 ppm
- OffsetError: 13 ppm + 21 ppm · 1 + 60 ppm = 94 ppm
- NoiseUncertainty: $\frac{315\,\mu V \quad 3}{\sqrt{10,000}}$ = 9.4 µV
- AbsoluteAccuracy: 10 V · (GainError) + 10 V · (OffsetError) + NoiseUncertainty = 1,660 µV

Analog Output

Number of channels	4
DAC resolution	16 bits
DNL	±1 LSB

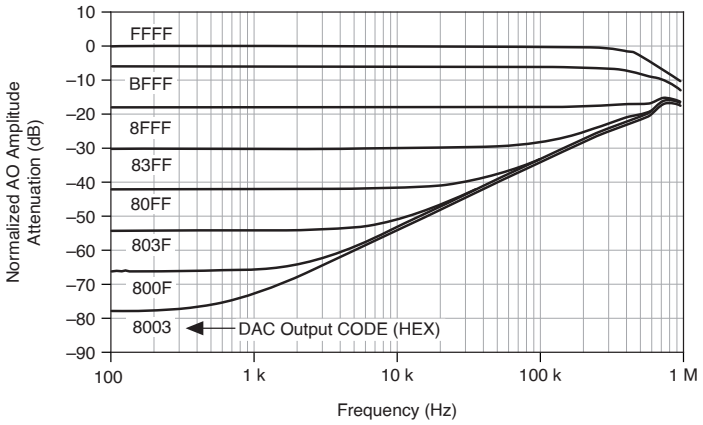
Monotonicity	16 bit guaranteed
Maximum update rate (simultaneous)	
1 channel	2.86 MSample/s
2 channels	2.00 MSample/s
3 channels	1.54 MSample/s
4 channels	1.25 MSample/s
Timing accuracy	50 ppm of sample rate
Timing resolution	10 ns
Output range	±10 V, ±5 V, ±external reference on APFI <0,1>
Output coupling	DC
Output impedance	0.2 Ω
Output current drive	±5 mA
Overdrive protection	±25 V
Overdrive current	26 mA
Power-on state	±5 mV
Power-on/off glitch	1.5 V peak for 200 ms
Output FIFO size	8,191 samples shared among channels used

Data transfers	DMA (scatter-gather), programmed I/O
AO waveform modes	Non-periodic waveform, periodic waveform regeneration mode from onboard FIFO, periodic waveform regeneration from host buffer including dynamic update
Settling time, full-scale step 15 ppm (1 LSB)	2 µs
Slew rate	20 V/µs
Glitch energy at midscale transition, ±10 V range	10 nV · s

External Reference

APFI <0,1> characteristics	
Input impedance	10 kΩ
Coupling	DC
Protection, device on	±30 V
Protection, device off	±15 V
Range	±11 V
Slew rate	20 V/µs

Figure 4. AO <0..3> External Reference Bandwidth



AO Absolute Accuracy (Warranted)

Table 3. AO Absolute Accuracy

Nominal Range Positive Full Scale (V)	Nominal Range Negative Full Scale (V)	Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco (ppm/°C)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/ °C)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale (µV)
10	-10	63	17	1	33	2	64	1,890
5	-5	70	8	1	33	2	64	935

Note **Absolute Accuracy at Full Scale** numbers are valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration.

Note Accuracies listed are valid for up to two years from the device external calibration.

AO Absolute Accuracy Equation

AbsoluteAccuracy = OutputValue · (GainError) + Range · (OffsetError)

- GainError = ResidualGainError + GainTempco · (TempChangeFromLastInternalCal) + ReferenceTempco · (TempChangeFromLastExternalCal)
- OffsetError = ResidualOffsetError + OffsetTempco · (TempChangeFromLastInternalCal) + INLError

Digital I/O/PFI

Static Characteristics

Number of channels	48 total, 32 (P0.<0..31>),16 (PFI <0..7>/P1, PFI <8..15>/P2)
Ground reference	D GND
Direction control	Each terminal individually programmable as input or output
Pull-down resistor	
Typical	50 kΩ
Minimum	20 kΩ
Input voltage protection	±20 V on up to two pins

Caution Stresses beyond those listed under the **Input voltage protection** specification may cause permanent damage to the device.

Waveform Characteristics (Port 0 Only)

Terminals used	Port 0 (P0.<0..31>)
Port/sample size	Up to 32 bits

Waveform generation (DO) FIFO	2,047 samples
Waveform acquisition (DI) FIFO	255 samples
DI Sample Clock frequency	0 MHz to 10 MHz, system and bus activity dependent
DO Sample Clock frequency	
Regenerate from FIFO	0 MHz to 10 MHz
Streaming from memory	0 MHz to 10 MHz, system and bus activity dependent
Data transfers	DMA (scatter-gather), programmed I/O
Digital line filter settings	160 ns, 10.24 µs, 5.12 ms, disable

PFI/Port1/Port 2 Functionality

Functionality	Static digital input, static digital output, timing input, timing output
Timing output sources	Many AI, AO, counter, DI, DO timing signals
Debounce filter settings	90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

Recommended Operating Conditions

Input high voltage (V_{IH})	
Minimum	2.2 V

Maximum	5.25 V
Input low voltage (V_{IL})	
Minimum	0 V
Maximum	0.8 V
Output high current (I_{OH})	
P0.<0..31>	-24 mA maximum
PFI <0..15>/P1/P2	-16 mA maximum
Output low current (I_{OL})	
P0.<0..31>	24 mA maximum
PFI <0..15>/P1/P2	16 mA maximum

Digital I/O Characteristics

Positive-going threshold (VT+)	2.2 V maximum
Negative-going threshold (VT-)	0.8 V minimum
Delta VT hysteresis (VT+ - VT-)	0.2 V minimum
I_{IL} input low current (V_{IN} = 0 V)	-10 µA maximum
I_{IH} input high current (V_{IN} = 5 V)	250 µA maximum

Figure 5. P0.<0..31>: I_{OH} versus V_{OH}

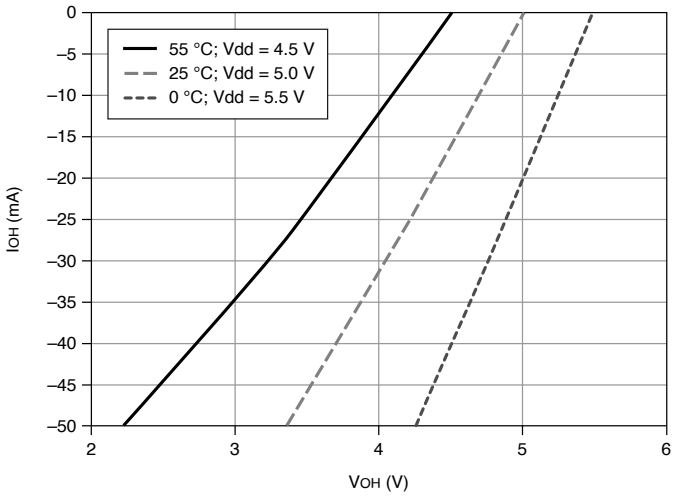


Figure 6. P0.<0..31>: I_{OL} versus V_{OL}

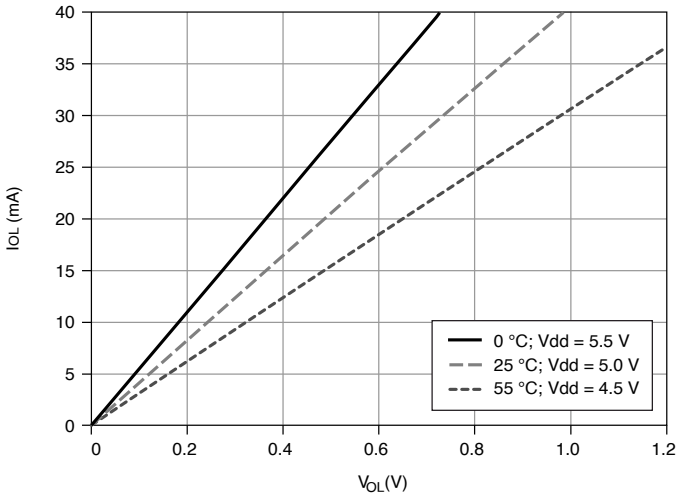


Figure 7. PFI <0..15>/P1/P2: I_{OH} versus V_{OH}

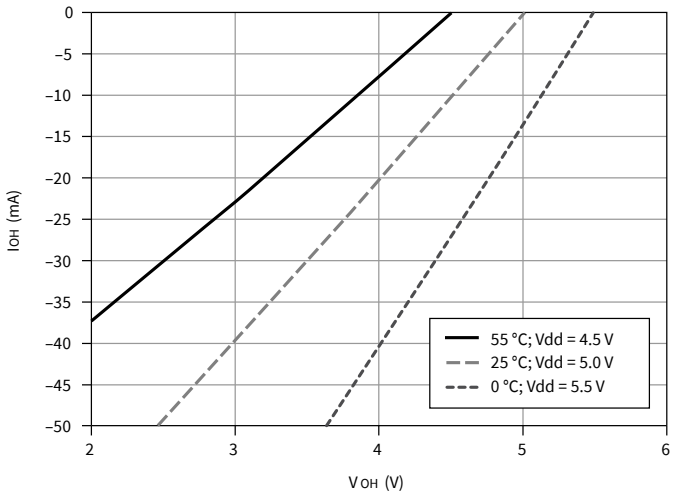
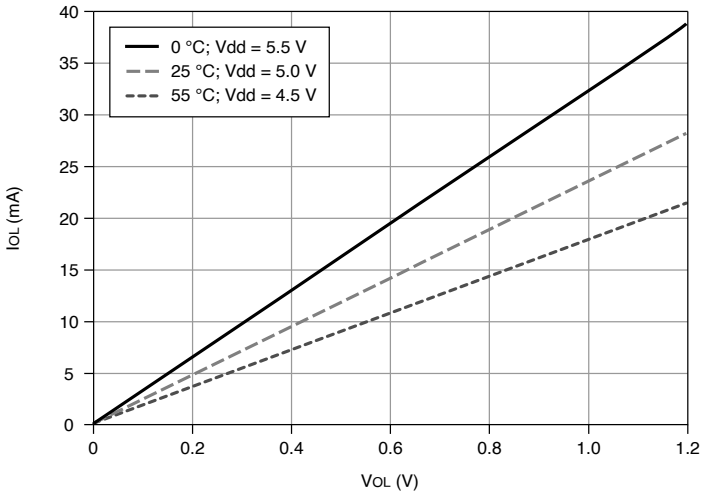


Figure 8. PFI <0..15>/P1/P2: I_{OL} versus V_{OL}



General-Purpose Counters

Number of counter/timers	4
Resolution	32 bits
Counter measurements	Edge counting, pulse, pulse width, semi-period, period, two-edge separation

Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	100 MHz, 20 MHz, 100 kHz
External base clock frequency	0 MHz to 25 MHz; 0 MHz to 100 MHz on PXIe_DSTAR <A,B>
Base clock accuracy	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Routing options for inputs	Any PFI, PXIe_DSTAR<A,B>, PXI_TRIG, PXI_STAR, analog trigger, many internal signals
FIFO	127 samples per counter
Data transfers	Dedicated scatter-gather DMA controller for each counter/timer, programmed I/O

Frequency Generator

Number of channels	1
Base clocks	20 MHz, 10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm

Phase-Locked Loop (PLL)

Number of PLLs	1
Reference clock locking frequency	
PXIe_DSTAR<A,B>	10 MHz, 20 MHz, 100 MHz
PXI_STAR	10 MHz, 20 MHz
PXIe_CLK100	100 MHz
PXI_TRIG <0..7>	10 MHz, 20 MHz
PFI <0..15>	10 MHz, 20 MHz
Output of PLL	100 MHz Timebase; other signals derived from 100 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source	Any PFI, PXIe_DSTAR<A,B>, PXI_TRIG,PXI_STAR
Polarity	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase

Counter/timer functions	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Digital waveform generation (DO) function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Digital waveform acquisition (DI) function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase

Device-to-Device Trigger Bus

Input source	PXI_TRIG <0..7>, PXI_STAR, PXIe_DSTAR<A,B>
Output destination	PXI_TRIG <0..7>, PXIe_DSTARC
Output selections	10 MHz Clock; frequency generator output; many internal signals
Debounce filter settings	90 ns, 5.12 µs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

Bus Interface

Form factor	x1 PXI Express peripheral module, specification rev 1.0 compliant
Slot compatibility	x1 and x4 PXI Express or PXI Express hybrid slots
DMA channels	8, can be used for analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3

Power Requirements

Caution The protection provided by the device can be impaired if the device is used in a manner not described in the **X Series User Manual**.

+3.3 V	1.6 W
+12 V	19.8 W

Current Limits

Caution Exceeding the current limits may cause unpredictable device behavior.

+5 V terminal (connector 0)	1 A maximum[1]
+5 V terminal (connector 1)	1 A maximum[1]
P0/PFI/P1/P2 and +5 V terminals combined	2 A maximum

Physical Characteristics

Printed circuit board dimensions	Standard 3U PXI
Weight	215 g (7.6 oz)
I/O connectors	
Module connector	68-Pos Right Angle Dual Stack PCB-Mount VHDCI (Receptacle)

Cable connector	68-Pos Offset IDC Cable Connector (Plug) (SHC68-*)

Note For more information about the connectors used for DAQ devices, refer to the document, **NI DAQ Device Custom Cables, Replacement Connectors, and Screws**, by going to ni.com/info and entering the Info Code rdspmb.

Calibration

Recommended warm-up time	15 minutes
Calibration interval	2 years

Maximum Working Voltage

Maximum working voltage refers to the signal voltage plus the common-mode voltage.

Channel to earth	11 V, Measurement Category I

Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as **MAINS** voltage. MAINS is a hazardous live electrical supply system that powers equipment. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.

Caution Do not connect the system to signals or use for measurements within Measurement Categories II, III, or IV.

Note Measurement Categories CAT I and CAT O are equivalent. These test and measurement circuits are for other circuits not intended for direct connection to the MAINS building installations of Measurement Categories CAT II, CAT III, or CAT IV.

Environmental

Temperature and Humidity

Temperature	
Operating	0 °C to 55 °C
Storage	-40 °C to 71 °C
Humidity	
Operating	10% to 90% RH, noncondensing
Storage	5% to 95% RH, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m

Indoor use only.

Shock and Vibration

Refer to the **X Series User Manual** for more information about meeting these specifications.

Operational shock	30 g peak, half-sine, 11 ms pulse
Random vibration	

Operating	5 Hz to 500 Hz, 0.3 g_{rms}
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms}

Environmental Standards

This product meets the requirements of the following environmental standards for electrical equipment.

- IEC 60068-2-1 Cold
- IEC 60068-2-2 Dry heat
- IEC 60068-2-27 Operating shock
- IEC 60068-2-64 Random operating vibration
- IEC 60068-2-56 Damp heat (steady state)
- MIL-PRF-28800F
  - Low temperature limits for operation Class 3, for storage Class 3
  - High temperature limits for operation Class 2, for storage Class 3
  - Random vibration for non-operating Class 3
  - Shock for operating Class 2

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility Standards

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

Notice For EMC declarations and certifications, and additional information, refer to the Product Certifications and Declarations section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2011/65/EU; Restriction of Hazardous Substances (RoHS)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- **中国 RoHS**— NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

PXIe-4141 Specifications

2024-01-05

Contents

PXIe-4141 Specifications. 3

PXIe-4141 Specifications

These specifications apply to the PXIe-4141.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are **Warranted** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature[1] of 23 °C ± 5 °C
- Calibration interval of 1 year
- 30 minutes warm-up time
- Self-calibration performed within the last 24 hours
- niDCPower Aperture Time property or NIDCPOWER_ATTR_APERTURE_TIME attribute set to 2 power-line cycles (PLC)
- Fans set to the highest setting if the PXI Express chassis has multiple fan speed settings

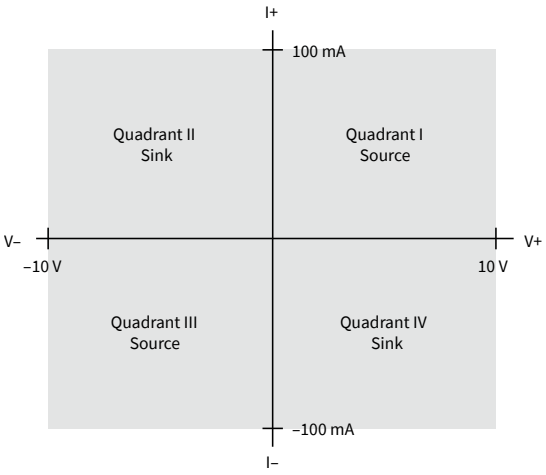
Device Capabilities

The following table and figure illustrate the voltage and the current source and sink ranges of the PXIe-4141.

Table 1. Current Source and Sink Ranges

Channels	DC Voltage Ranges	DC Current Source and Sink Ranges
0 through 3	±10 V	▪ 10 µA ▪ 100 µA ▪ 1 mA ▪ 10 mA ▪ 100 mA

Figure 1. Quadrant Diagram, All Channels



SMU Specifications

Voltage Programming and Measurement Accuracy/ Resolution

Table 2. Voltage Programming and Measurement Accuracy/Resolution

Range	Resolution and noise (0.1 Hz to 10 Hz)	Accuracy (23 °C ± 5 °C) ± (% of voltage + offset) [2]		Tempco ± (% of voltage + offset)/°C, 0 °C to 55 °C
		T_{cal} ± 5 °C	T_{cal} ± 1 °C	
10 V	10 µV	0.015% + 600 µV	0.013% + 150 µV	0.0005% + 1 µV

Related tasks:

- Calculating SMU Resolution

Related reference:

- Additional Specifications

Current

Table 3. Current Programming and Measurement Accuracy/Resolution

Range	Resolution and noise (0.1 Hz to 10 Hz)	Accuracy (23 °C ± 5 °C) ± (% of current + offset)		Tempco ± (% of current + offset)/°C, 0 °C to 55 °C
		T_{cal} ± 5 °C	T_{cal} ± 1 °C	
10 µA	10 pA	0.03% + 1.5 nA	0.03% + 300 pA	0.002% + 10 pA
100 µA	100 pA	0.03% + 15 nA	0.03% + 3.0 nA	0.002% + 100 pA
1 mA	1 nA	0.03% + 150 nA	0.03% + 30 nA	0.002% + 1.0 nA
10 mA	10 nA	0.03% + 1.5 µA	0.03% + 300 nA	0.002% + 10 nA
100 mA	100 nA	0.03% + 15 µA	0.03% + 3.0 µA	0.002% + 100 nA

Related tasks:

- Calculating SMU Resolution

Related reference:

- Additional Specifications

Output Resistance Programming Accuracy/Resolution, Typical

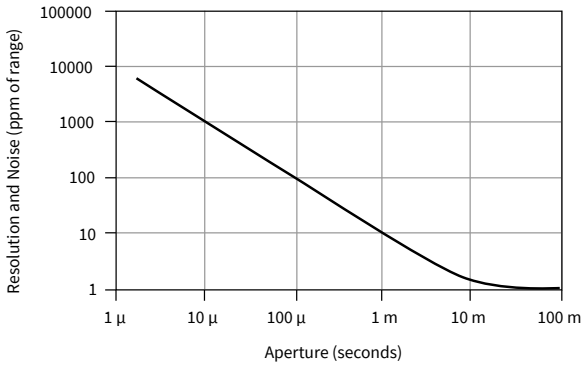
Table 4. Output Resistance Programming Accuracy/Resolution, Typical

Current limit range	Programmable resistance range	Resolution	Accuracy ± (% of resistance setting), T_{cal} ± 5 °C
10 µA	± 100 kΩ	1 Ω	0.04% + 510 mΩ
100 µA	± 10 kΩ	100 mΩ	0.04% + 60 mΩ
1 mA	± 1 kΩ	10 mΩ	0.04% + 15 mΩ
10 mA	± 100 Ω	1 mΩ	0.04% + 10 mΩ
100 mA	± 10 Ω	100 µΩ	0.04% + 10 mΩ

Calculating SMU Resolution

Refer to the following figure as you complete the following steps to derive a resolution in absolute units:

Figure 1. Noise and Resolution versus Measurement Aperture, Typical



1. Select a voltage or current range.
2. For a given aperture time, find the corresponding resolution.
3. To convert resolution from ppm of range to absolute units, multiply resolution in ppm of range by the selected range.

Example of Calculating SMU Resolution

The PXIe-4141 has a resolution of 100 ppm when set to a 100 µs aperture time. In the 10 V range, resolution can be calculated by multiplying 10 V by 100 ppm, as shown in the following equation:

$10\ V * 100\ ppm = 10\ V * 100 * 1\times10^{-6} = 1\ mV$

Likewise, in the 100 mA range, resolution can be calculated by multiplying 100 mA by 100 ppm, as shown in the following equation:

$100\ mA * 100\ ppm = 100\ mA * 100 * 1\times10^{-6} = 10\ \mu A$

Additional Specifications

Settling time[3]	<100 µs to settle to 0.1% of voltage step, device configured for fast transient response, typical
Transient response	<100 µs to recover within ±20 mV after a load current change from 10% to 90% of range, device configured for fast transient response, typical
Wideband source noise[4]	1.5 mV RMS, typical <20 $mV_{pk\text{-}pk}$, typical
Cable guard output impedance	10 kΩ, typical
Remote sense	
Voltage	Add 0.1% of LO lead drop to voltage accuracy specification
Current	Add 0.02% of range per volt of total HI and LO lead drop to current accuracy specification

Maximum lead drop	Up to 1 V drop per lead
Load regulation	
Voltage	10 µV at connector pins per mA of output load when using local sense, typical
Current	20 pA + (10 ppm of range per volt of output change) when using local sense, typical
Isolation voltage, channel-to-earth ground	60 VDC, CAT I, verified by dielectric withstand test, 5 s, continuous, characteristic
Absolute maximum voltage between any terminal and LO	20 VDC, continuous

The following figures illustrate the effect of the transient response setting on the step response of the PXIe-4141 for different loads.

Figure 1. 1 mA Range No Load Step Response, Typical

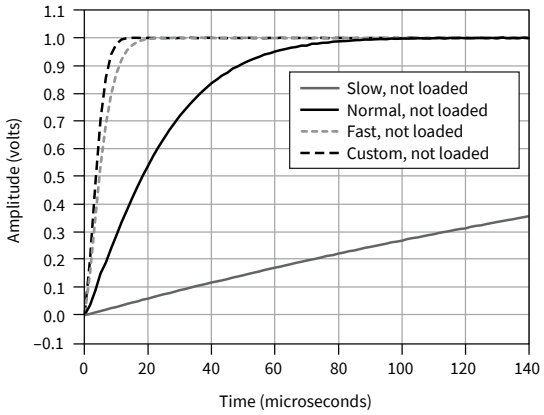
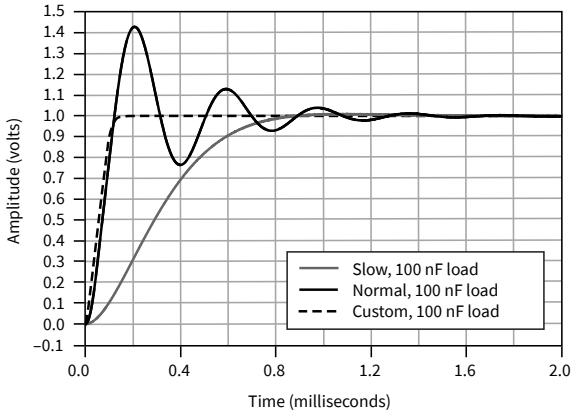


Figure 1. 1 mA Range, 100 nF Load Step Response, Typical



Related reference:

- Voltage Programming and Measurement Accuracy/Resolution
- Current

Supplemental Specifications

Measurement and Update Timing

Available sample rates[5]	(600 kS/s)/N

where

- N = 6, 7, 8, … 2^{20}
- S is samples

Sample rate accuracy	±50 ppm
Maximum measure rate to host[6]	600,000 S/s per channel, continuous
Maximum source update rate[7]	
Sequence length <300 steps per iteration	100,000 updates/s per channel

Sequence length ≥300 steps per iteration	100,000 updates/s per board
Input trigger to	
Source event delay	5 µs
Source event jitter	1.7 µs
Measure event jitter	1.7 µs

Triggers

Input triggers	
Types	Start Source Sequence Advance Measure
Sources (PXI trigger lines 0 to 7)[]	
Polarity	Active high (not configurable)
Minimum pulse width	100 ns
Destinations[9] **(PXI trigger lines 0 to 7)**[]	
Polarity	Active high (not configurable)
Minimum pulse width	200 ns
Output triggers (events)	
Types	Source Complete

	Sequence Iteration Complete Sequence Engine Done Measure Complete
Destinations (PXI trigger lines 0 to 7)[]	
Polarity	Active high (not configurable)
Pulse width	230 ns

Calibration Interval

Recommended calibration interval	1 year

Physical

Dimensions	3U, one-slot, PXI Express/CompactPCI Express module 2.0 cm × 13.0 cm × 21.6 cm (0.8 in. × 5.1 in. × 8.5 in.)
Weight	
20 W	425 g (14.99 oz)
40 W	428 g (15.1 oz)
Front panel connectors	25-position D-SUB, male

Power Requirement

PXIe-4141 (40W)	3.0 A from the 3.3 V rail and 6.0 A from the 12 V rail
PXIe-4141 (20W)	2.5 A from the 3.3 V rail and 2.7 A from the 12 V rail

Environmental Characteristics

Temperature	
Operating	0 °C to 55 °C
Storage	
Humidity	
Operating	10% to 70%, noncondensing. Derate 1.3% per °C above 40 °C.
Storage	5% to 95%, noncondensing.
Pollution Degree	2
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse

PXIe-6571

2024-01-05

Contents

PXIe-6571 Specifications. 3

PXIe-6571 Specifications

These specifications apply to the PXIe-6571. When using the PXIe-6571 in the Semiconductor Test System, refer to the **Semiconductor Test System Specifications**.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

The following characteristic specifications describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Operating temperature of 0 °C to 40 °C
- Chassis with 82 W slot cooling capacity
- Operating temperature within ±5 °C of the last self-calibration temperature [1]
- Recommended calibration interval of 1 year. The PXIe-6571 will not meet specifications unless operated within the recommended calibration interval.
- DUT Ground Sense (DGS) same potential as the Ground (GND) pins

- 30-minute warmup time before operation

Note When the pin electronics on the PXIe-6571 are in the disconnect state, some I/O protection and sensing circuitry remain connected. Do not subject the PXIe-6571 to voltages beyond the supported measurement range.

General

Channel count	32
Multi-site resources per instrument	8
System channel count[2]	512
Large Vector Memory (LVM)	128M vectors
History RAM (HRAM)	(8,192/N sites)-1 cycles
Maximum allowable offset (DGS minus GND)	±300 mV
Supported measurement range[3]	-2 V to 7 V[4]

Timing

Vector Timing

Maximum vector rate	100 MHz
Vector period range	10 ns to 40 µs (100 MHz to 25 kHz)
Vector period resolution	38 fs

Timing control	
Vector period	Vector-by-vector on the fly
Edge timing	Per channel, vector-by-vector on the fly
Drive formats	Per channel, vector-by-vector on the fly

Clocking

Master clock source	PXIe_CLK100[5]
Sequencer clock domains	One (independent sequencer clock domains on a single instrument not supported)

Drive and Compare Formats

Drive formats[6]	
100 MHz maximum vector rate	Non-Return (NR), Return to Low (RL), Return to High (RH)
50 MHz maximum vector rate	Surround by Complement (SBC)[7]
Compare formats	Edge strobe
Edge Multipliers[6]	1x, 2x

Figure 1. Drive Formats

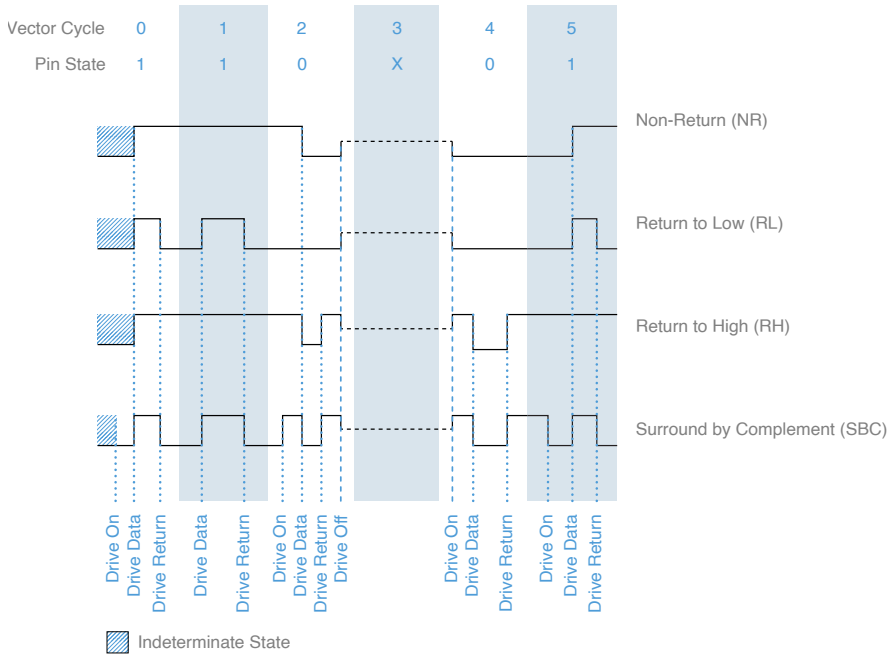
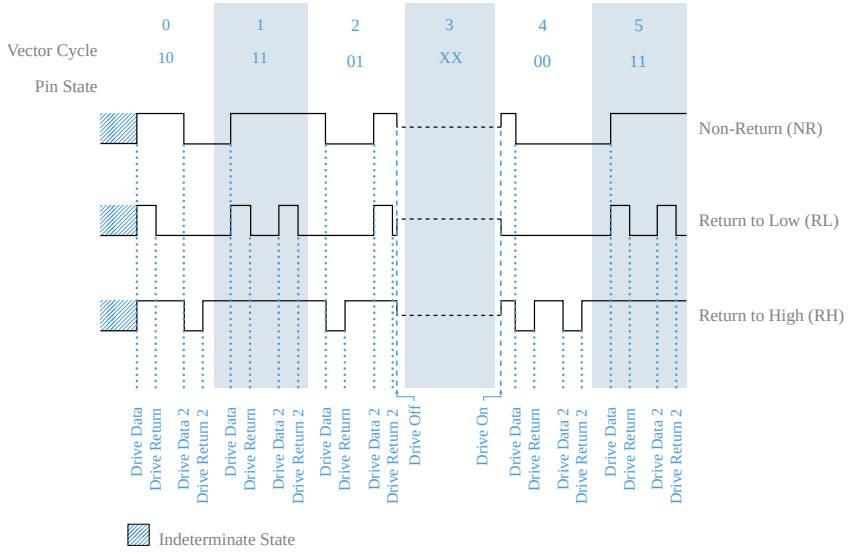


Figure 2. 2x Mode Drive Formats



Pin Data States

Pin States

- 0 — Drive zero.

- 1 — Drive one.
- L — Compare low.
- H — Compare high.
- X — Do not drive; mask compare.
- M — Compare midband, not high or low.
- V — Compare high or low, not midband; store results from capture functionality if configured.
- D — Drive data from source functionality if configured.
- E — Expect data from source functionality if configured.
- - — Repeat previous cycle. Do not use a dash (-) for the pin state on the first vector of a pattern file unless the file is used only as a target of a jump or call operation.

Note Termination mode settings affect the termination applied to all non-driving pin states. Non-drive states include L, H, M, V, X, E, and potentially -. Refer to the Programmable input termination mode specification for more information.

Edge Timing

Edge Types

Drive edges	6; drive on, drive data, drive return, drive data 2, drive return 2, drive off
Compare edge	2; strobe, strobe 2
Number of time sets[8]	31

Edge Generation Timing

Edge placement range

Minimum	Start of vector period (0 ns)
Maximum	5 vector periods or 40 µs, whichever is smaller
Minimum required edge separation	
Between any driven data change	3.75 ns
Between any Drive On and Drive Off edges	5 ns
Between Compare Strobes	5 ns
Edge placement resolution	39.0625 ps
Edge placement accuracy[9]	
Drive	
Edge Multiplier = 1x	±500 ps, warranted
Edge Multiplier = 2x	Bit rate ≤ 200 Mbps: ±500 ps, typical
Edge Multiplier = 2x	Bit rate ≤ 266 Mbps: ±600 ps, typical
Compare	
Edge Multiplier = 1x	±500 ps, warranted
Edge Multiplier = 2x	Bit rate ≤ 100 Mbps: ±500 ps, typical
Edge Multiplier = 2x	Bit rate ≤ 133 Mbps: ±700 ps, typical
Overall timing accuracy[9]	
Edge Multiplier = 1x	±1.5 ns, warranted

Edge Multiplier = 2x	Bit rate ≤ 200 Mbps: ±1.5 ns, typical
Edge Multiplier = 2x	Bit rate ≤ 266 Mbps: ±1.8 ns, typical
TDR deskew adjustment resolution	39.0625 ps

Driver, Comparator, Load

Driver

Signal type	Single-ended, referenced to the DGS pin when connected. Otherwise referenced to GND.
Programmable levels	V_{IH}, V_{IL}, V_{TERM}
Voltage levels	
Range (V_{IH}, V_{IL}, V_{TERM})	-2 V to 6 V
Minimum swing (V_{IH} minus V_{IL})	400 mV, into a 1 MΩ load
Resolution (V_{IH}, V_{IL}, V_{TERM})	122 µV
Accuracy (V_{IH}, V_{IL}, V_{TERM})	±15 mV, 1 MΩ load, warranted
Maximum DC drive current	±32 mA
Output impedance	50 Ω
Rise/fall time, 20% to 80%	1.2 ns, up to 5 V

Comparator

Signal type	Single-ended, referenced to the DGS pin when connected. Otherwise referenced to GND.
Programmable levels	V_{OH}, V_{OL}
Voltage levels	
Range (V_{OH}, V_{OL})	-2 V to 6 V
Resolution (V_{OH}, V_{OL})	122 µV
Accuracy (V_{OH}, V_{OL})	±25 mV, from -1.5 V to 5.8 V, warranted
Programmable input termination modes	High Z, 50 Ω to V_{TERM}, Active Load
Leakage current	<15 nA, in the High Z termination mode

Active Load

Programmable levels	I_{OH}, I_{OL}
Commutating voltage (V_{COM})	
Range	-2 V to 6 V
Resolution	122 µV
Current levels	
Range	1.5 mA to 16 mA
Resolution	488 nA

Accuracy	1 mA, 3 V over/under drive, typical

PPMU

PPMU Force Voltage

Signal type	Single-ended, referenced to the DGS pin when connected. Otherwise referenced to GND.
Voltage levels	
Range	-2 V to 6 V 6 V to 7 V in Extended Voltage Range[10]
Resolution	122 µV
Accuracy	±15 mV, 1 MΩ load, from -2 V to 6 V, warranted ±50 mV, 1 MΩ load, from 6 V to 7 V, typical[10]

PPMU Measure Voltage

Signal type	Single-ended, referenced to the DGS pin when connected. Otherwise referenced to GND.
Voltage levels	
Range	-2 V to 6 V
Resolution	228 µV
Accuracy	±5 mV, warranted

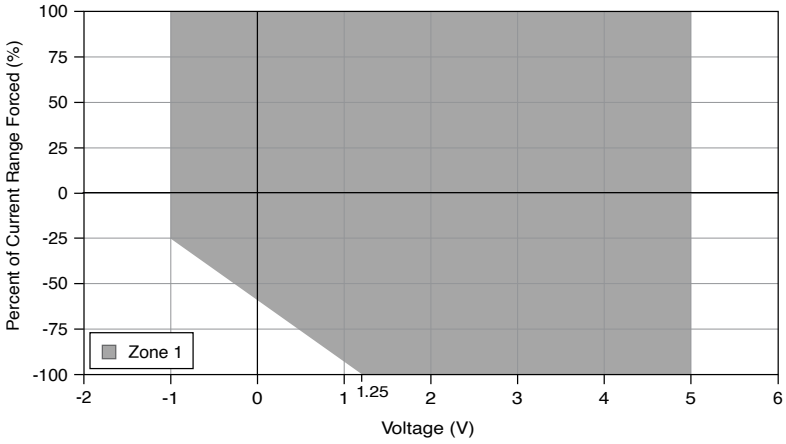
PPMU Force Current

How to Calculate PPMU Force Current Accuracy

Table 1. PPMU Force Current Accuracy

Range	Resolution	Accuracy
±2 µA	60 pA	±1% of range for Zone 1 of Figure 3, warranted
±32 µA	980 pA	
±128 µA	3.9 nA	
±2 mA	60 nA	
±32 mA	980 nA	

Figure 3. Warranted Current Accuracy Zone for PPMU Force Current



Note The boundaries of Zone 1 are inclusive of that zone. The area outside of Zone 1 does not have a warranted spec for PPMU force current accuracy.

1. Specify the desired forced current.
2. Based on the desired forced current, select an appropriate current range from Table 1.
3. Divide the desired forced current from step 1 by the current range from step 2 and multiply by 100 to calculate the Percent of Current Range Forced.

4. Based on the impedance of the load, calculate the voltage required to force the desired current from step 1. Use the following equation: Voltage Required = Desired Current * Load Impedance.
5. Using Figure 2, locate the zone in which the Percent of Current Range Forced calculated in step 3 intersects with the Voltage calculated in step 4. If the intersection is outside of Zone 1, then there are no warranted specs. To get warranted specs, the current range and/or forced current must be adjusted until the intersection is in Zone 1.
6. Based on the zone found in step 5, use Table 1 to calculate the accuracy of the forced current.

PPMU voltage clamps	
Range	-2 V to 6 V
Resolution	122 µV
Accuracy	±100 mV, typical

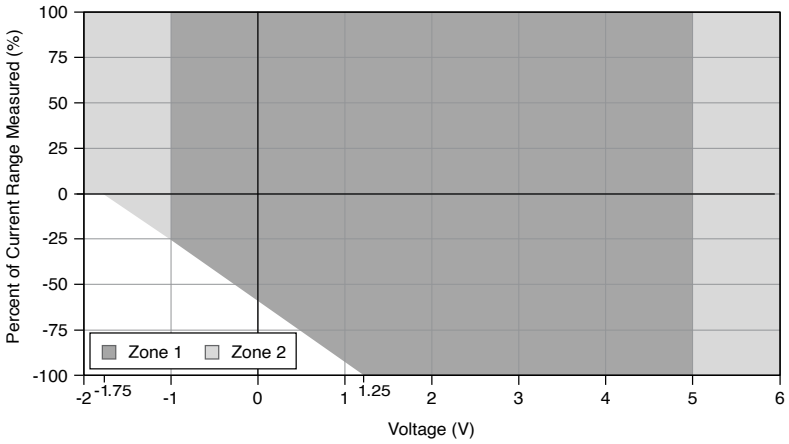
PPMU Measure Current

How to Calculate PPMU Measure Current Accuracy

Table 2. PPMU Measure Current Accuracy

Range	Resolution	Accuracy
±2 µA	460 pA	±1% of range for Zone 1 of Figure 4, warranted ±1.5% of range for Zone 2 of Figure 4, warranted
±32 µA	7.3 nA	
±128 µA	30 nA	
±2 mA	460 nA	
±32 mA	7.3 µA	

Figure 4. Warranted Current Accuracy Zones for PPMU Measure Current



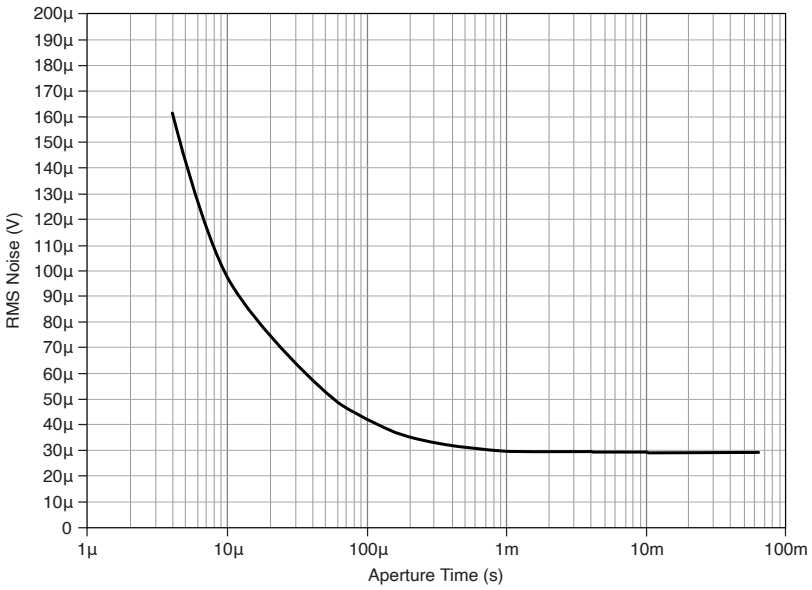
Note The boundaries of Zone 1 are inclusive of that zone. All other boundaries are inclusive of Zone 2. The area outside of Zone 1 and Zone 2 does not have a warranted spec for PPMU measure current accuracy.

1. Specify the desired measured current.
2. Based on the desired measured current, select an appropriate current range from Table 2.
3. Divide the desired measured current from step 1 by the current range from step 2 and multiply by 100 to calculate the Percent of Current Range Measured.
4. If forcing voltage and then measuring current, Voltage in Figure 3 is equal to the forced voltage. If forcing current and then measuring current, Voltage in Figure 3 is equal to the voltage required to force the desired current based on the impedance of the load. Use the following equation: Voltage Required = Desired Current * Load Impedance.
5. Using Figure 3, locate the zone in which the Percent of Current Range Measured calculated in step 3 intersects with the Voltage calculated in step 4. If the intersection is outside of Zone 1 or Zone 2, then there are no warranted specs. To get warranted specs, the current range and forced current or forced voltage must be adjusted until the intersection is in Zone 1 or Zone 2.
6. Based on the zone found in step 5, use Table 2 to calculate the accuracy of the measured current.

PPMU Programmable Aperture Time

Aperture time	
Minimum	4 µs
Maximum	65 ms
Resolution	4 µs

Figure 5. Voltage Measurement Noise for Given Aperture Times, Typical



Pattern Control

Opcodes

Refer to the following table for supported opcodes. Using matched and failed opcode parameters with multiple PXIe-6571 instruments requires the PXIe-6674T synchronization module. Other uses of flow-control opcodes with multiple PXIe-6571 instruments only require NI-TCLK synchronization.

Category	Supported Opcodes
Flow Control	▪ repeat ▪ jump ▪ jump_if ▪ set_loop ▪ end_loop ▪ exit_loop ▪ exit_loop_if ▪ call ▪ return ▪ keep_alive ▪ match ▪ halt
Sequencer Flags and Registers	▪ set_seqflag ▪ clear_seqflag ▪ write_reg
Signal	▪ set_signal ▪ pulse_signal ▪ clear_signal
Digital Source and Capture	▪ capture_start ▪ capture ▪ capture_stop ▪ source_start ▪ source ▪ source_d_replace

Pipeline Latencies

Minimum delay between source_start opcode and the first source opcode or subsequent source_start opcode	3 µs
Matched and failed condition pipeline latency	80 cycles

Source and Capture

Digital Source[11]	
Operation modes	Serial and parallel; broadcast and site-unique
Source memory size	32 MB (256 Mbit) total
Maximum waveforms	512
Digital Capture[11]	
Operation modes	Serial and parallel; site-unique
Capture memory size	1 million samples
Maximum waveforms	512

Independent Clock Generators

Number of Clock Generators	32 (one per pin)
Clock Period Range	6.25 ns to 40 us (160 MHz to 25 kHz)[12]
Clock Period Resolution	38 fs

Frequency Measurements

Frequency counter measure frequency	
Range	5 kHz to 200 MHz, 2.5 ns minimum pulse width
Accuracy	See Calculating Frequency Counter Error

Calculating Frequency Counter Error

Use the following equation to calculate the frequency counter error (ppm).

$$\left(\frac{TB_{err}}{(1 - TB_{err})} + \frac{20ns}{(MeasurementTime - UnknownClockPeriod)}\right) * 1,000,000$$

where

- MeasurementTime is the time, in seconds, over which the frequency counter measurement is configured to run
- UnknownClockPeriod is the time, in seconds, of the period of the signal being measured
- TB_{err} is the error of the Clk100 timebase

Refer to the following table for a few examples of common Clk100 timebase accuracies.

Table 3. TB_{err}

PXI Express Hardware Specification Revision 1.0	PXIe-1095 Chassis	PXIe-6674T Override
100 µ (100 ppm)	25 µ (25 ppm)	80 n (80 ppb)

Example 1: Calculating Error with a PXIe-1095 Chassis

Calculate the error of performing a frequency measurement of a 10 MHz clock (100 ns period) with a 1 ms measurement time using the PXIe-Clk100 provided by the PXIe-1095 chassis as the timebase.

Solution

$$\left(\frac{25\mu}{(1 - 25\mu)} + \frac{20ns}{(1ms - 100ns}\right) * 1,000,000$$

$$= 45ppm$$

Example 2: Calculating Error when Overriding with the PXIe-6674T

Calculate the error if you override the PXIe-Clk100 timebase with the PXIe-6674T and increase the measurement time to 10 ms.

Solution

$$\left(\frac{80n}{(1 - 80n)} + \frac{20ns}{(10ms - 100ns}\right) * 1,000,000$$

$$= 2ppm$$

Calibration Interval

Recommended calibration interval	1 year

Physical Characteristics

PXIe slots	1

Dimensions	131 mm × 21 mm × 214 mm (5.16 in. × 0.83 in. × 8.43 in.)
Weight	640 g (22.5 oz.)

Power Requirements

The PXIe-6571 draws current from a combination of the 3.3 V and 12 V power rails. The maximum current drawn from each of these rails can vary depending on the PXIe-6571 mode of operation.

Input power	76 W
Current Draw	
3.3 V	1.7 A
12 V	5.9 A

PXIe-5163 Specifications

2024-01-05

Contents

PXIe-5163 Specifications. 3

PXIe-5163 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Nominal** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges, bandwidths, and bandwidth-limiting filters
- Sample rate set to 1 GS/s
- Onboard sample clock locked to onboard reference clock
- 15-minute warm-up time at ambient temperature

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 50 °C
- Calibration cycle maintained
- Chassis configured:[1]
  - PXI Express chassis fan speed set to HIGH
  - Foam fan filters removed if present
  - Empty slots contain PXI chassis slot blockers and filler panels
- External calibration performed at 23 °C ± 3 °C
- Within ±5 °C of temperature at last self-calibration as reported by onboard temperature sensor

Typical specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 50 °C

Vertical

Analog Input

Number of channels	Two (simultaneously sampled)
Input type	Referenced single-ended
Connectors	BNC, ground referenced

Impedance and Coupling

Input impedance	50 Ω ±1.25%, typical 1 MΩ ±0.5%, typical
Input capacitance (1 MΩ)	20.2 pF ±2.5 pF, typical

Input coupling	AC DC

Figure 1. 50 Ω Voltage Standing Wave Ratio (VSWR)

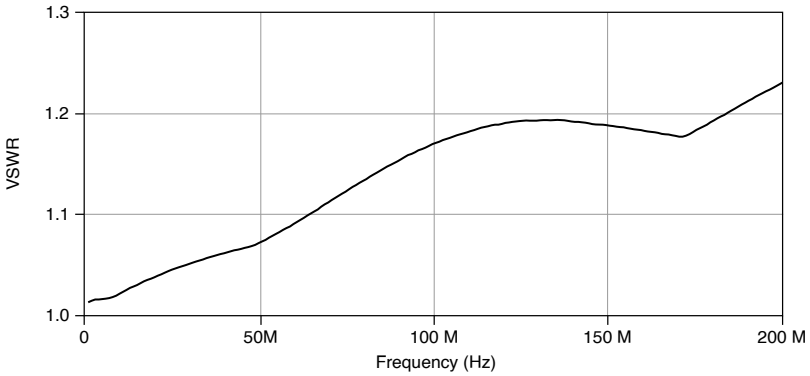
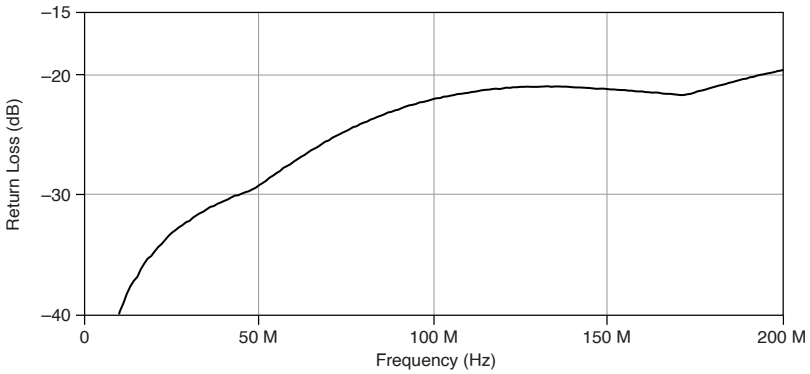


Figure 1. 50 Ω Input Return Loss



Voltage Levels

50 Ω FS input range (V_{pk-pk})	0.25 V 0.5 V 1 V 2.5 V 5 V

Table 1. 1 MΩ FS Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	Vertical Offset Range[2] (V)
0.25 V	±5
0.5 V	±5
1 V	±5
2.5 V	±10 or ±248.75
5 V	±10 or ±247.5
10 V	±10 or ±245
25 V	±50 or ±237.5
50 V	±50 or ±225
100 V	±50 or ±200
Maximum input overload	
50 Ω	|Peaks| ≤5 V
1 MΩ [3]	250 V RMS

Notice Signals exceeding the maximum input overload may cause damage to the device.

Accuracy

Resolution	14 bits
DC accuracy[4], [5]	
50 Ω	±[(0.5% × |**Reading**|) + (0.2% of FS)], warranted
1 MΩ	±[(0.65% × |**Reading** - **Vertical Offset**|) + (0.4% × |**Vertical Offset**|) + (0.2% of FS) + 0.15 mV], warranted

DC drift[6]	±0.0013 dB per °C at 50 kHz
AC amplitude accuracy[4]	±0.225 dB at 50 kHz, warranted

Crosstalk Crosstalk is measured on one channel with a test signal applied to the other channel and the same range setting on both channels.

Table 2. 50 Ω Crosstalk

Frequency	Level
1 MHz	-100 dB
10 MHz	-100 dB
100 MHz	-85 dB
200 MHz	-75 dB

Table 3. 1 MΩ Crosstalk

Frequency	Level	
	0.25 V to 10 V (V_{pk-pk})	25 V to 100 V (V_{pk-pk})
1 MHz	-85 dB	-70 dB
10 MHz	-85 dB	-70 dB
100 MHz	-75 dB	-55 dB
200 MHz	-70 dB	-50 dB

Bandwidth and Transient Response

Bandwidth (-3 dB)[7],[8]	200 MHz, warranted
Bandwidth-limiting filters[7],[8]	
Lowpass filters	20 MHz 30 MHz

	150 MHz
Highpass filters	90 Hz 450 Hz
Passband amplitude flatness (at <150 MHz)[7],[8]	
50 Ω	±0.5 dB, warranted
1 MΩ	±0.7 dB, typical
AC-coupling cutoff (-3 dB)	
50 Ω [9]	40 kHz
1 MΩ [8]	7.5 Hz
Rise/fall time[10]	2 ns

Figure 1. 50 Ω Full Bandwidth Frequency Response, 1 $V_{pk\text{-}pk}$, Measured

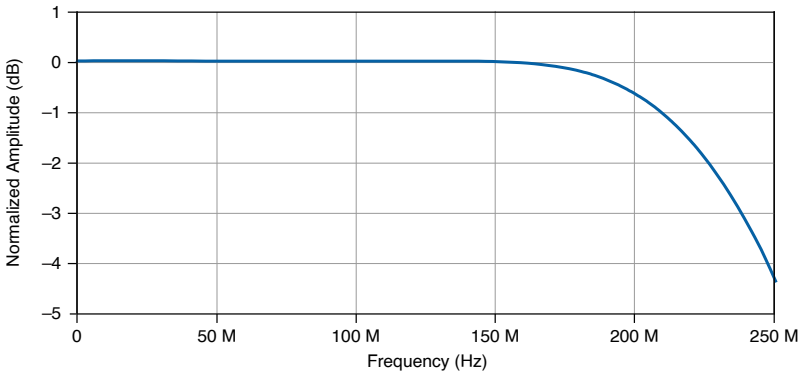


Figure 1. 50 Ω Full Bandwidth Frequency Response Zoomed, 1 V_{pk-pk}, Measured

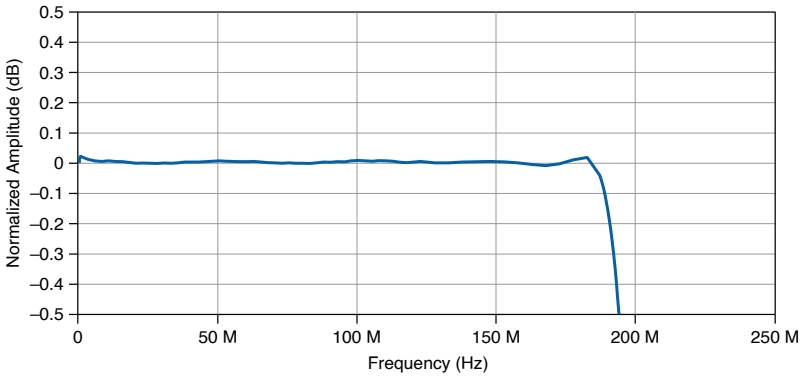


Figure 1. 50 Ω 150 MHz Bandwidth Frequency Response, 1 V_{pk-pk}, Measured

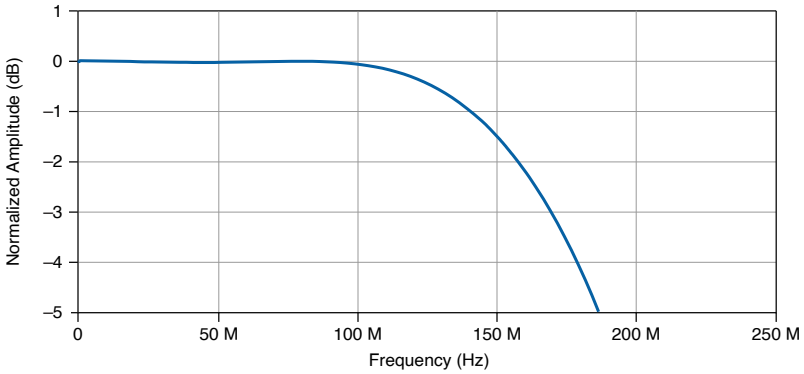


Figure 1. 1 MΩ Full Bandwidth Frequency Response, 1 V_{pk-pk}, Measured

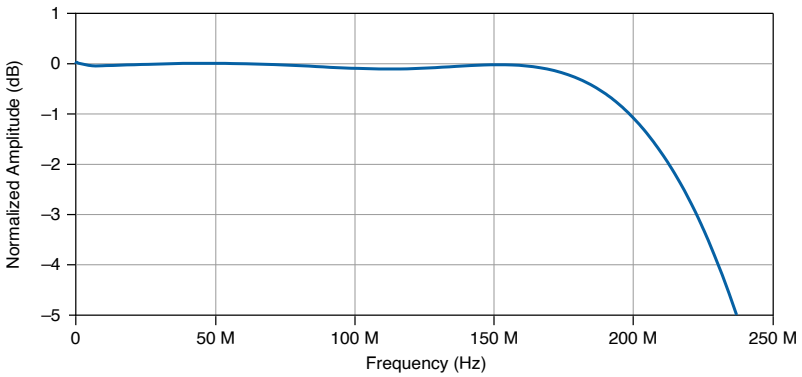


Figure 1. 1 MΩ Full Bandwidth Frequency Response Zoomed, 1 V_{pk-pk}, Measured

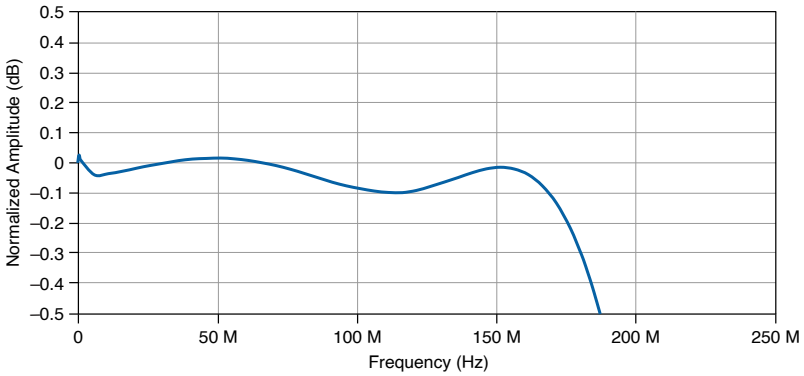
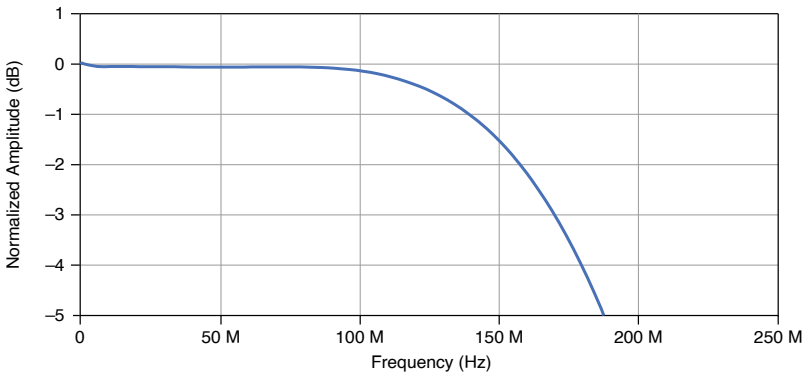


Figure 1. 1 MΩ 150 MHz Bandwidth Frequency Response, 1 V_{pk-pk}, Measured



Spectral Characteristics

50 Ω Spectral Characteristics Excludes ADC interleaving spurs. 1

Table 4. Spurious-Free Dynamic Range (SFDR)[11]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)
0.25 V	-70
0.5 V	-73
1 V	-73
2.5 V	-73
5 V	-70

Table 5. Total Harmonic Distortion (THD)[12]

Input Range (V_{pk-pk})	<50 MHz, Full Bandwidth (dBc)	≥50 MHz to ≤100 MHz, Full Bandwidth (dBc)
0.25 V	-73	-69
0.5 V	-73	-72
1 V	-72	-70
2.5 V	-72	-68
5 V	-72	-69

Table 6. Effective Number of Bits (ENOB)[11]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth	<100 MHz, 150 MHz Filter
0.25 V	10.5	10.7
0.5 V	10.7	10.9
1 V	10.7	11.0
2.5 V	10.9	11.1
5 V	10.8	11.0

Figure 1. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk} Input Range, 150 MHz Filter, 9.9 MHz Input Tone at -1 dBFS, Measured

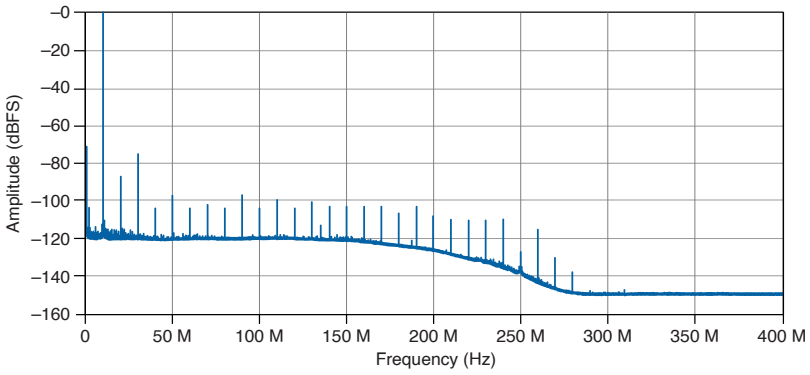


Figure 1. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Measured

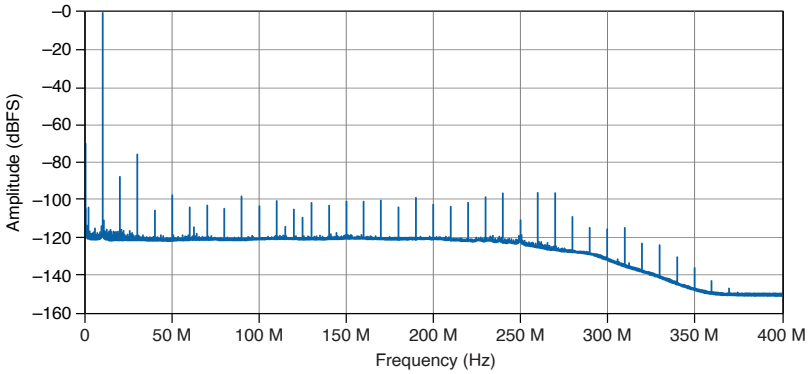
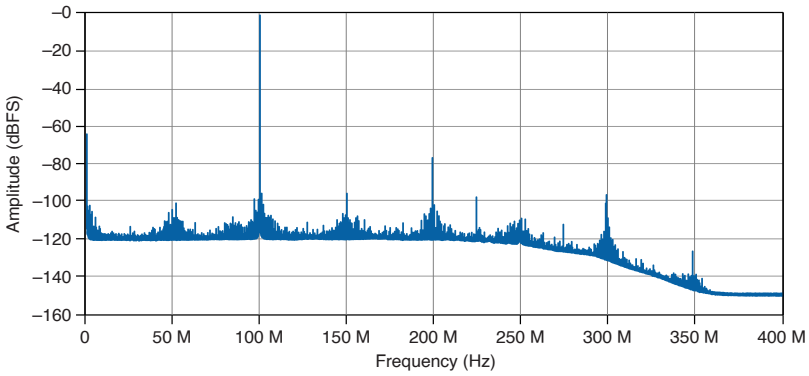


Figure 1. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 99.9 MHz Input Tone at -1 dBFS, Measured



1 MΩ Spectral Characteristics 1 , Verified using a 50 Ω source and 50 Ω feed-through terminator.

Figure 1. 1 MΩ Single-Tone Spectrum, 1 V_{pk-pk} Input Range, 150 MHz Filter, 9.9 MHz Input Tone at -1 dBFS, Measured

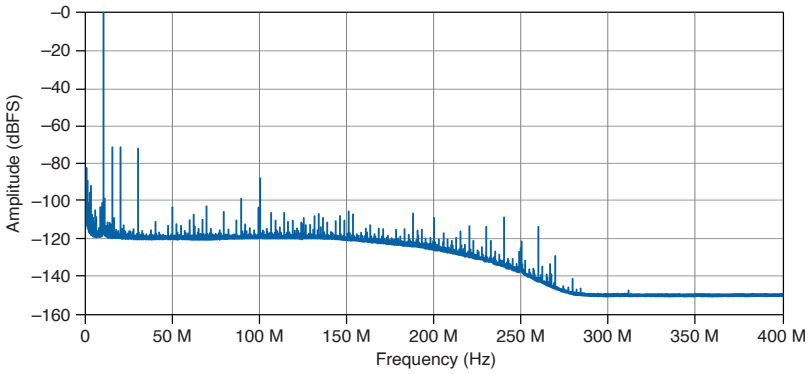
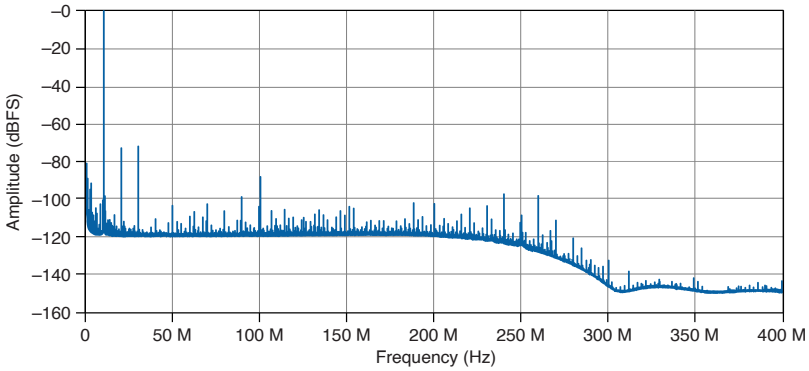


Figure 1. 1 MΩ Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Measured



Noise[13]

50 Ω RMS Noise

Input Range (V_{pk-pk})	RMS Noise (% of FS)	
	Full Bandwidth, Warranted	150 MHz Filter, Typical
0.25 V	0.045	0.018
0.5 V	0.040	0.018
1 V	0.035	0.017
2.5 V	0.030	0.017
5 V	0.030	0.014

Figure 1. 50 Ω Channel 0 Average Noise Density, 1 V_{pk-pk} Range, Measured

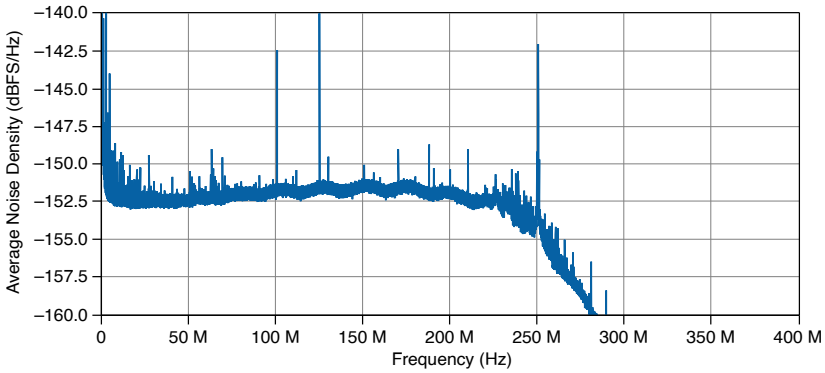
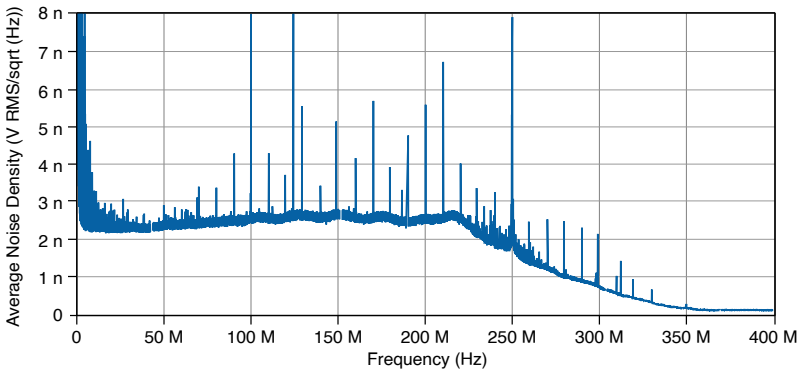


Figure 1. 50 Ω Channel 0 Average Noise Density, 0.25 V_{pk-pk} Range, Measured



1 MΩ RMS Noise

Input Range (V_{pk-pk})	RMS Noise (% of FS)	
	Full Bandwidth, Warranted	150 MHz Filter, Typical
0.25 V	0.110	0.070
0.5 V	0.060	0.050
1 V	0.050	0.030
2.5 V	0.100	0.055
5 V	0.060	0.045
10 V	0.050	0.030
25 V	0.080	0.050

Input Range (V_{pk-pk})	RMS Noise (% of FS)	
	Full Bandwidth, Warranted	150 MHz Filter, Typical
50 V	0.060	0.040
100 V	0.050	0.030

Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCTCXO)
External	CLK IN (front panel SMB connector) PXIe-DSTAR_A (backplane connector)
Sample rate range, real-time[14]	15.259 kS/s to 1 GS/s
Timebase frequency	1.0 GHz
Timebase accuracy	
Phase-locked to onboard clock	±5 ppm, warranted
Phase-locked to external clock	Equal to the external clock accuracy
Sample clock jitter[15]	500 fs RMS

Phase-Locked Loop (PLL) Reference Clock

Sources	
Internal	Onboard clock (internal VCTCXO)

	PXI_CLK10 (backplane connector)
External (10 MHz)	CLK IN (front panel SMB connector) AUX 0 CLK IN (front panel MHDMR connector)
Duty cycle tolerance	45% to 55%, typical

External Sample Clock

Source	CLK IN (front panel SMB connector)
Impedance	50 Ω
Coupling	AC
Frequency	1.0 GHz
Input voltage range, when configured as a sample clock	632 mV_{pk-pk} to 5 V_{pk-pk} (0 dBm to 18 dBm), typical
Maximum input overload, when configured as a sample clock	6 V_{pk-pk}
Duty cycle tolerance	45% to 55%, typical

External Reference Clock In

Sources	CLK IN (front panel SMB connector) AUX 0 CLK IN (front panel MHDMR connector)

Impedance	50 Ω
Coupling	AC
Frequency[16]	10 MHz
Input voltage range, when configured as a reference clock	623 mV_{pk-pk} to 5 V_{pk-pk} (0 dBm to 18 dBm), typical
Maximum input overload, when configured as a reference clock	6 V_{pk-pk}

Reference Clock Out

Source	PXI_CLK10 (backplane connector)
Destination	AUX 0 CLK OUT (front panel MHDMR connector)
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	±12 mA

Trigger

Supported triggers	Reference (stop) trigger Reference (arm) trigger Start trigger

	Advance trigger
Trigger types	Edge Window Hysteresis Digital Immediate Software
Trigger sources	CH 0 CH 1 SMB PFI 0 AUX 0 PFI <0..7> PXI_Trig <0..6> Software
Trigger delay	from 0 ns to 2.25×10^{15} ns ($(2^{51} - 1) \times$ **Sample Clock Period** ns)
Dead time	496 ns
Hold off	From dead time to 1.84×10^{19} ns ($(2^{64} - 1) \times$ **Sample Clock Period** ns)

Analog Trigger

Sources	CH 0 CH 1
Time resolution	
Interpolator enabled	**Sample Clock Period** / 1024 = 0.977 ps
Interpolator disabled	Sample clock period (1 ns)
Trigger filters	
Low Frequency (LF) Reject	100 kHz
High Frequency (HF) Reject	100 kHz
Trigger accuracy[17]	0.5% of FS
Trigger jitter[17]	15 ps RMS
Minimum threshold duration[18]	Sample clock period

Digital Trigger

Sources	PFI 0 (front panel SMB connector) AUX 0 PFI <0..7> (front panel MHDMR connector) PXI_Trig <0..6> (backplane connector)
Time resolution	8 ns

Programmable Function Interface

Connectors	AUX 0 PFI <0..7> (front panel MHDMR connector) PFI 0 (front panel SMB connector)
Direction	Bidirectional per channel
As an input (trigger)	
Destination	Start trigger (acquisition arm) Reference (stop) trigger Arm reference trigger Advance trigger
Input impedance	49.9 kΩ
V_{IH}	2 V, typical
V_{IL}	0.8 V, typical
Recommended input range	3.3 V
Maximum input overload	0 to 3.3 V (5 V tolerant)
Maximum frequency	50 MHz
Minimum pulse width	10 ns
As an output (event)	
Sources	Ready for Start

	Start trigger (acquisition arm) Ready for Reference Reference (stop) trigger End of Record Ready for Advance Advance trigger Done (end of acquisition) Probe compensation[19]
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	12 mA
Maximum frequency	50 MHz
Minimum pulse width	10 ns

AUX 0 Connector Specifications

Connector	MHDMR
Voltage output	3.3 V ±10%
Maximum current drive on +3.3 V	200 mA

Output impedance on +3.3 V	<1 Ω

Waveform Specifications

Onboard memory size[20]	512 MB
Minimum record length	1 sample
Number of pretrigger samples	Zero up to (**Record Length** - 1)
Number of posttrigger samples	Zero up to **Record Length**
Maximum number of records in onboard memory[21]	1,398,101 for 512 MB

Table 10. Examples of Allocated Onboard Memory Per Record (512 MB Onboard Memory)

Channels	Bytes per Sample	Max Records per Channel	Record Length	Allocated Onboard Memory per Record
1	2	1,398,101	1	384
1	2	223,696	1,000	2,400
1	2	26,379	10,000	20,352
1	2	1	268,435,265	536,870,912
2	2	1,398,101	1	384
2	2	121,574	1,000	4,416
2	2	13,283	10,000	33,216
2	2	1	134,217,633	536,870,912

Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, which is available at ni.com/manuals.

Calibration

External Calibration

External calibration yields the following benefits:

- Corrects for gain and offset errors of the onboard references used in self-calibration.
- Adjusts timebase accuracy.
- Compensates the 1 MΩ ranges.
- Corrects the frequency response for all ranges.

All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for the following aspects:

- Gain
- Offset
- Interleaving spurs
- Intermodule synchronization errors

Refer to the **NI High-Speed Digitizers Help** for information about when to self-calibrate the device.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[22]	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE18.7.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-5163. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can use InstrumentStudio to monitor, control, and record measurements from the PXIe-5163.

InstrumentStudio is an application that allows you to perform interactive measurements on several different NI device types in a single application.

Interactive control of the PXIe-5163 was first available via InstrumentStudio in NI-SCOPE18.7. InstrumentStudio is included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5163. MAX is included on the driver media.

Synchronization

Channel-to-channel skew, between the channels of a PXIe-5163	
50 Ω	<100 ps
1 MΩ	<150 ps

Note The channels of a PXIe-5163 are automatically synchronized when they are in the same NI-SCOPE session.

Synchronization with the NI-TClk API [23]

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PXIe-5163 and NI-SCOPE.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

Module-to-module skew, between PXIe-5163 modules using NI-TClk [24]	
NI-TClk synchronization without manual adjustment [25]	
Skew, peak-to-peak [26]	300 ps, typical
NI-TClk synchronization with manual adjustment [25]	
Skew, average	≤10 ps
Sample Clock delay/adjustment resolution	3.5 ps

Power Requirements

Current draw

+3.3 V DC	1.97 A
+12 V DC	1.63 A
Power draw	
+3.3 V DC	6.5 W
+12 V DC	19.5 W
Total	26 W

Physical

Dimensions	3U, one-slot, PXI Express Gen 2 x8 module 21.26 cm × 12.88 cm × 2.0 cm (8.37 in. × 5.07 in. × 0.787 in.)
Weight	460 g (16.2 oz)

Bus Interface

Form factor	PXI Express (x8 Gen 2)
Slot compatibility	PXI Express or hybrid

Environmental Characteristics

Temperature	
Operating	0 °C to 50 °C

Storage	-40 °C to 71 °C
Humidity	
Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing
Pollution Degree	2
Maximum altitude	4,600 m (570 mbar) (at 25 °C ambient temperature)
Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

PCI-5142 Specifications

2024-01-05

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PCI-5142 Specifications. 3

PCI-5142 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Typical** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All filter settings
- All impedance selections
- Sample clock set to 100 MS/s

Vertical

Analog Input (Channel 0 and Channel 1)

Number of channels	Two (simultaneously sampled)
Connector	BNC

Impedance and Coupling

Input impedance (software-selectable)	50 Ω ± 2.0% 1 MΩ ± 0.75% in parallel with a nominal capacitance of 27 pF ± 2 pF
Input coupling (software-selectable)	AC[1] DC GND

Voltage Levels

Table 1. Full Scale (FS) Input Range and Programmable Vertical Offset

Range (V_{pk-pk})	Vertical Offset Range	
	50 Ω	1 MΩ
0.2 V	±0.1 V	
0.4 V	±0.2 V	
1 V	±0.5 V	
2 V	±1 V	
4 V	±2 V	
10 V	—	±5 V

Range (V_{pk-pk})	Vertical Offset Range	
	50 Ω	1 MΩ
20 V	—	—

Maximum input overload	
50 Ω	7 V RMS with |Peaks| ≤10 V
1 MΩ	|Peaks| ≤42 V

Accuracy

Resolution	14 bits

Table 2. DC Accuracy (Programmable Vertical Offset = 0 V)[2], Warranted

Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V and 0.4 V	±(0.65% of input + 2.0 mV)	
1 V	±(0.65% of input + 2.0 mV)	
2 V	±(0.65% of input + 2.2 mV)	
4 V	±(0.65% of input + 8.0 mV)	
10 V	±(0.65% of input + 10.0 mV)	
20 V	—	±(0.65% of input + 15.0 mV)

Programmable vertical offset accuracy[2]	±0.5% of offset setting

Table 3. DC Drift, Nominal

Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V, 0.4 V, 1 V, and 2 V	±(0.057% of Input + 0.006% of FS + 100 µV) per °C	
4 V, 10 V	±(0.057% of Input + 0.006% of FS + 900 µV) per °C	
20 V	—	±(0.057% of Input + 0.006% of FS + 900 µV) per °C

AC amplitude accuracy[2]

50 Ω	±0.06 dB (±0.7%) at 50 kHz
1 MΩ	±0.09 dB (±1.0%) at 50 kHz
Crosstalk[3]	≤-100 dB at 10 MHz

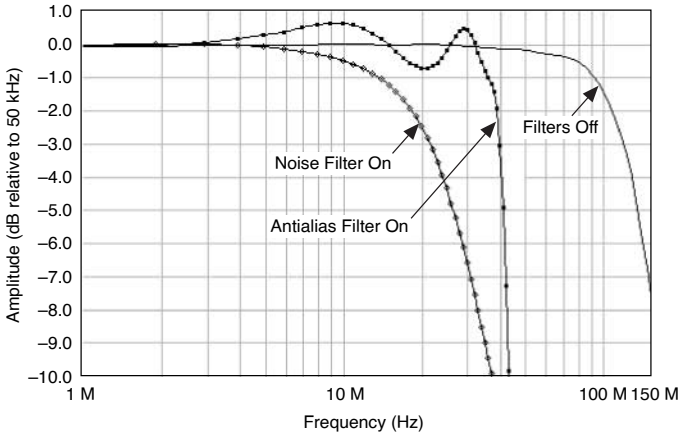
Bandwidth and Transient Response

Bandwidth (±3 dB, filters off)[4]	
0.2 V_{pk-pk} input range	80 MHz up to 40 °C, warranted[5]
All other input ranges	100 MHz, warranted
Rise/fall time	
0.2 V_{pk-pk} input range	4.2 ns
All other input ranges	3.5 ns
Bandwidth limit filters[6]	
Noise filter	20 MHz 2-pole Bessel filter
Anti-alias Filter	40 MHz (-6 dB) 35 MHz (±3 dB), warranted 6-pole Chebyshev filter
AC coupling cutoff (-3 dB)	12 Hz [7]

Table 4. Passband Flatness[4]

Filter Settings	Input Range (V_{pk-pk})	50 Ω and 1 MΩ
Filters off	0.2 V	±0.4 dB (DC to 20 MHz) ±1 dB (20 MHz to 40 MHz)
	All other input ranges	±0.4 dB (DC to 20 MHz) ±1 dB (20 MHz to 50 MHz)
Anti-alias filter on	All input ranges	±1.2 dB (DC to 16 MHz) ±1.6 dB (16 MHz to 32 MHz)

Figure 1. PCI-5142 Frequency Response, Measured



Spectral Characteristics

Table 5. Spurious-Free Dynamic Range (SFDR) with Harmonics[8]

Input Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V	75 dBc	70 dBc
0.4 V	75 dBc	70 dBc
1 V	75 dBc	70 dBc

Input Range (V_{pk-pk})	50 Ω	1 MΩ
2 V	75 dBc	70 dBc
4 V	65 dBc	70 dBc
10 V	65 dBc	60 dBc
20 V	—	60 dBc

Table 6. Total Harmonic Distortion (THD)[9]

Input Range (V_{pk-pk})	50 Ω	1 MΩ
0.2 V	-75 dBc	-68 dBc
0.4 V	-75 dBc	-68 dBc
1 V	-75 dBc	-68 dBc
2 V	-73 dBc	-68 dBc
4 V	-63 dBc	-68 dBc
10 V	-63 dBc	-58 dBc
20 V	—	-58 dBc

Intermodulation distortion[10]	-75 dBc

Table 7. Signal-to-Noise Ratio (SNR)[11]

Input Range (V_{pk-pk})	50 Ω		1 MΩ	
	Filters Off	Anti-alias Filter On	Filters Off	Anti-alias Filter On
0.2 V	60 dB	60 dB	56 dB	60 dB
0.4 V	62 dB	62 dB	61 dB	62 dB
1 V	62 dB	62 dB	62 dB	62 dB
2 V	62 dB	62 dB	62 dB	62 dB
4 V	—	—	61 dB	62 dB

Table 8. Signal to Noise and Distortion (SINAD)[12]

Input Range (V_{pk-pk})	50 Ω		1 MΩ	
	Filters Off	Anti-alias Filter On	Filters Off	Anti-alias Filter On
0.2 V	60 dB	60 dB	56 dB	59 dB
0.4 V	62 dB	62 dB	60 dB	61 dB

Input Range (V_{pk-pk})	50 Ω		1 MΩ	
	Filters Off	Anti-alias Filter On	Filters Off	Anti-alias Filter On
1 V	62 dB	62 dB	61 dB	61 dB
2 V	62 dB	62 dB	61 dB	61 dB
4 V	—	—	60 dB	61 dB

Figure 2. PCI-5142 Dynamic Performance, 50 Ω, 1 V Input Range, Measured

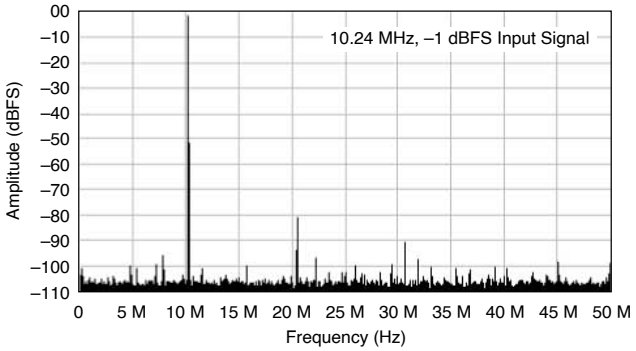


Table 9. RMS Noise (Noise Filter On)[13]

Input Range (V_{pk-pk})	50 Ω (V RMS)	1 MΩ (V RMS)
0.2 V	56 µV (0.028% of FS)	72 µV (0.036% of FS)
0.4 V	92 µV (0.023% of FS)	92 µV (0.023% of FS)
1 V	230 µV (0.023% of FS)	230 µV (0.023% of FS)
2 V	460 µV (0.023% of FS)	460 µV (0.023% of FS)
4 V	920 µV (0.023% of FS)	920 µV (0.023% of FS)
10 V	2.3 mV (0.023% of FS)	2.3 mV (0.023% of FS)
20 V	—	4.6 mV (0.023% of FS)

Table 10. RMS Noise (Anti-alias Filter On)[13]

Input Range (V_{pk-pk})	50 Ω (V RMS)	1 MΩ (V RMS)
0.2 V	82 µV (0.041% of FS)	96 µV (0.048% of FS)
0.4 V	100 µV (0.025% of FS)	120 µV (0.030% of FS)
1 V	250 µV (0.025% of FS)	300 µV (0.030% of FS)
2 V	500 µV (0.025% of FS)	600 µV (0.030% of FS)
4 V	1 mV (0.025% of FS)	1.2 mV (0.030% of FS)
10 V	2.5 mV (0.025% of FS)	3 mV (0.030% of FS)

Input Range (V_{pk-pk})	50 Ω (V RMS)	1 MΩ (V RMS)
20 V	—	6 mV (0.030% of FS)

Table 11. RMS Noise (Filters Off)[13]

Input Range (V_{pk-pk})	50 Ω (V RMS)	1 MΩ (V RMS)
0.2 V	90 µV (0.045% of FS)	110 µV (0.055% of FS)
0.4 V	100 µV (0.025% of FS)	160 µV (0.040% of FS)
1 V	250 µV (0.025% of FS)	300 µV (0.030% of FS)
2 V	500 µV (0.025% of FS)	600 µV (0.030% of FS)
4 V	1 mV (0.025% of FS)	1.6 mV (0.040% of FS)
10 V	2.5 mV (0.025% of FS)	3 mV (0.030% of FS)
20 V	—	6 mV (0.030% of FS)

Figure 3. PCI-5142 Spectral Noise Density on 0.2 V Input Range, Full Bandwidth, 50 Ω Input Impedance, Nominal

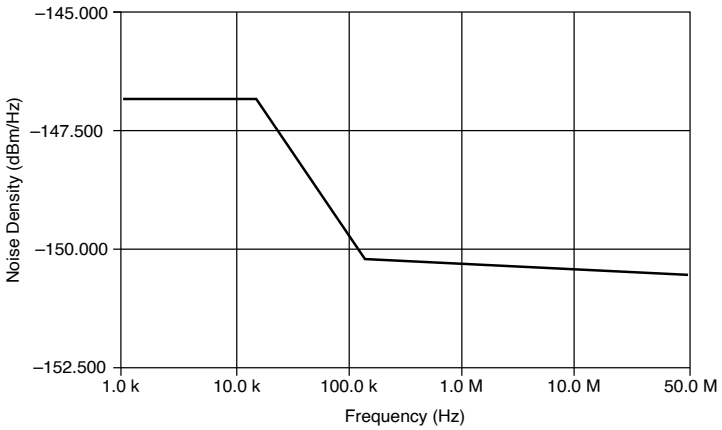
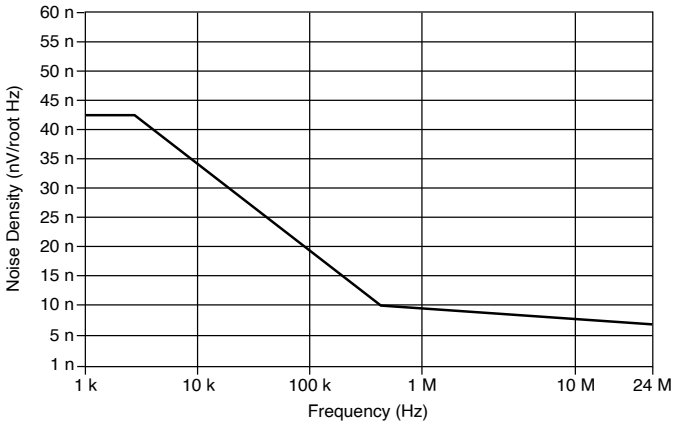


Figure 4. PCI-5142 Spectral Noise Density on 0.2 V Input Range, Noise Filter Enabled, 1 MΩ Input Impedance, Nominal



Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCXO)[14]
External	CLK IN (front panel SMB connector)

Onboard Clock (Internal VCXO)

Sample rate range	
Real-time sampling (single shot)	1.526 kS/s to 100 MS/s[15]
Random interleaved sampling (RIS)	200 MS/s to 2 GS/s in multiples of 100 MS/s
Phase noise density[16]	
100 Hz input frequency	<-100 dBc/Hz
1 kHz input frequency	<-120 dBc/Hz

10 kHz input frequency	<-130 dBc/Hz
Sample clock jitter[17]	≤1 ps RMS (100 Hz to 100 kHz) ≤2 ps RMS (100 Hz to 1 MHz)
Timebase frequency	100 MHz
Timebase accuracy	
Not phase-locked to Reference clock	±25 ppm, warranted
Phase-locked to Reference clock	Equal to the Reference clock accuracy
Sample clock delay range	±1 Sample clock period
Sample clock delay resolution	≤10 ps

Related information:

- For more information about the Sample clock and decimation, refer to the NI High-Speed Digitizers Help, available online at ni.com/manuals.

External Sample Clock

Source	CLK IN (front panel SMB connector)
Frequency range[18]	
CLK IN	30 MHz to 105 MHz
Duty cycle tolerance	45% to 55%

Related information:

- For more information about the Sample clock and decimation, refer to the NI High-Speed Digitizers Help, available online at ni.com/manuals.

Sample Clock Exporting

Table 12. Exported Sample Clock Destinations

Destination	Maximum Frequency
CLK OUT (front panel SMB connector)	105 MHz
PXI_Trig <0..6> (backplane connector)[19]	20 MHz
PFI <0..1> (front panel 9-pin mini-circular DIN connector)[19]	25 MHz
RTSI <0..6>[19]	20 MHz

Phase-Locked Loop (PLL) Reference Clock

Sources	RTSI 7 CLK IN (front panel SMB connector)
Frequency range	5 MHz to 20 MHz in 1 MHz increments[20]
Duty cycle tolerance	45% to 55%
Exported Reference clock destinations	CLK OUT (front panel SMB connector) PFI <0..1> (front panel 9-pin mini-circular DIN connector) RTSI <0..7>

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Input voltage range	
Sine wave (V_{pk-pk})	0.65 V to 2.8 V (0 dBm to 13 dBm)

Square wave (V_{pk-pk})	0.2 V to 2.8 V
Maximum input overload[21]	7 V RMS with |Peaks| ≤10 V
Impedance	50 Ω
Coupling	AC

CLK OUT (Sample Clock and Reference Clock Output, Front Panel Connector)

Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum drive current	±48 mA

Trigger

Reference (Stop) Trigger

Trigger types	Edge Window Hysteresis Video Digital Immediate

	Software
Trigger sources	CH 0 CH 1 TRIG PXI_Trig <0..6> PFI <0..1> PXI Star Trigger Software RTSI <0..6>

Note Refer to the following sections and the **NI High-Speed Digitizers Help** for more information about what sources are available for each trigger type.

Table 13. Time Resolution

Time-to-Digital Conversion Circuit (TDC)	Onboard Clock	External Clock
On	100 ps	—
Off	10 ns	External clock period

Table 14. Minimum Rearm Time[22]

TDC	Rearm Time
On	10 µs
Off	2 µs

Table 15. Holdoff

TDC	Onboard Clock	External Clock
On	10 µs to 171.79 s	—
Off	2 µs to 171.79 s	200 × **External Clock Period** to (2^{32} - 1) × **External Clock Period**

Analog Trigger

Trigger types	Edge Window Hysteresis
Sources	CH 0 (front panel BNC connector) CH 1 (front panel BNC connector) TRIG (front panel BNC connector)
Trigger level range	
CH 0, CH 1	100% of FS
TRIG (external trigger)	±5 V
Trigger level resolution	10 bits (1 in 1,024)
Edge trigger sensitivity, warranted	
CH 0, CH 1	2.5% of FS up to 50 MHz Increases to 5% of FS at 100 MHz
TRIG (external trigger, V_{pk-pk})	0.25 V up to 100 MHz

	Increases to 1 V at 200 MHz
Level accuracy	
CH 0, CH 1	±3.5% of FS up to 10 MHz
TRIG (external trigger)	±0.35 V (±3.5% of FS) up to 10 MHz
Jitter	≤80 ps RMS [23]
Trigger filters	
Low-frequency (LF) reject	50 kHz
High-frequency (HF) reject	50 kHz

Digital Trigger

Trigger type	Digital
Sources	RTSI <0..6> PFI <0..1> (front panel 9-pinmini-circular DIN connector)

Video Trigger

Trigger type	Video
Sources	CH 0 (front panel BNC connector) CH 1 (front panel BNC connector) TRIG (front panel BNC connector)

Video trigger types	Specific Line Any Line Specific Field
Standard	Negative sync of NTSC, PAL, or SECAM signal

External Trigger

Connector	TRIG (front panel BNC connector)
Impedance	1 MΩ in parallel with 22 pF
Coupling	AC, DC
AC coupling cutoff (-3 dB)	12 Hz
Input voltage range	±5 V
Maximum input overload	|Peaks| ≤42 V

PFI 0 and PFI 1 (Programmable Function Interface)

Connector	AUX I/O (9-pin mini-circular DIN)
Direction	Bidirectional
As an Input (Trigger)	
Destinations	Start trigger (acquisition arm) Reference (stop) trigger

	Arm Reference trigger Advance trigger
Input impedance	150 kΩ, nominal
V_{IH}	2.0 V
V_{IL}	0.8 V
Maximum input overload	-0.5 V to 5.5 V
Maximum frequency	25 MHz
As an Output (Event)	
Sources	Ready for Start Start trigger (acquisition arm) Ready for Reference Reference (stop) trigger End of Record Ready for Advance Advance trigger Done (end of acquisition) Probe Compensation[24]
Output impedance	50 Ω

Logic type	3.3 V CMOS
Maximum drive current	±24 mA
Maximum frequency	25 MHz

Waveform Specifications

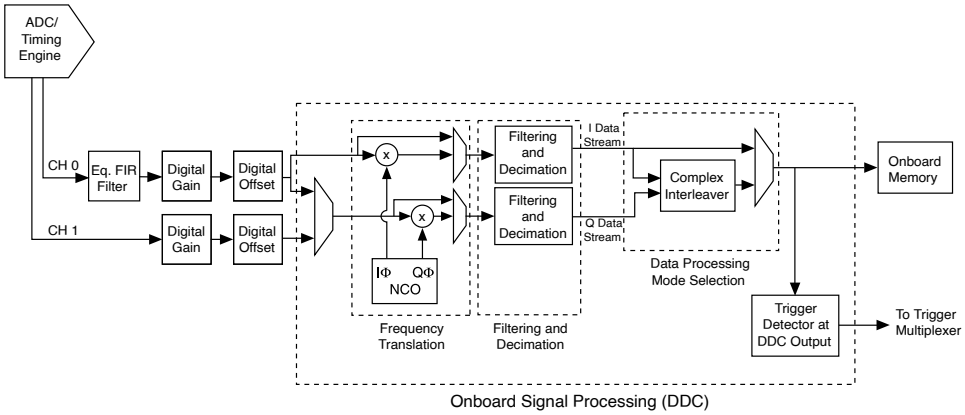
Onboard memory size	
64 MB per channel option	32 MS per channel[25]
256 MB per channel option	128 MS per channel[25]
Minimum record length	1 sample
Number of pretrigger samples	Zero up to full record length[26]
Number of posttrigger samples	Zero up to full record length[26]
Maximum number of records in onboard memory	
64 MB/channel	100,000[27]
256 MB/channel	100,000[27]
Allocated onboard memory per record	
Real data processing mode	(**Record Length** × 2 bytes/S) + 200 bytes, rounded up to next multiple of either 128 bytes or 512 bytes, whichever is greater
Complex data processing mode	(**Record Length** × 4 bytes/S) + 200 bytes, rounded up to next multiple of either 128 bytes or 512 bytes, whichever is greater

Related information:

- For more information about the Sample clock and decimation, refer to the NI High-Speed Digitizers Help, available online at ni.com/manuals.

Onboard Signal Processing (OSP)

Figure 5. PCI-5142 Onboard Signal Processing Block Diagram



Note To use onboard signal processing (OSP) on the PCI-5142, the DDC Enabled property/attribute must be set to TRUE.

The following four OSP operations are available:

- Send one IF signal to CH 0 and perform quadrature downconversion on the signal (complex data is returned).
- Send I and Q baseband signals to CH 0 and CH 1 and perform alias-protected decimation (complex data is returned).
- Send a signal to CH 0 and perform alias-protected decimation (real data is returned).
- Send a signal to CH 0 and perform real downconversion on the signal (real data is returned).

Number of digital downconverters (DDCs)	1

Data processing modes[28]	Real (I path only) Complex (IQ)
OSP decimation range[29]	1, 2, 4, 6, 8, 10 12 to 4,096 (multiples of 4) 4,096 to 8,192 (multiples of 8) 8,192 to 16,384 (multiples of 16)
Sample rate range[30]	
Internal Sample clock timebase	6.1 kS/s to 100 MS/s (real or complex)
External Sample clock timebase	Sample clock timebase/OSP decimation
Real flat bandwidth	0.4 × **Sample Rate**
Complex flat bandwidth[31]	0.8 × **Sample Rate**

Digital Gain and Offset

Digital gain and offset resolution	18 bits
Digital gain range	-1.5 to +1.5 |Values| < 1 attenuate user data
Digital offset range	(-0.4 × **Vertical Range**) to (+0.4 × **Vertical Range**)[32]
Output	(**ADC Data** × **Digital Gain**) + **Digital Offset**.[33]

Numerically-Controlled Oscillator (NCO)

Frequency range[34]	
Internal Sample clock timebase	0 Hz to 50 MHz
External Sample clock timebase	0 Hz to (0.5 × **Sample Clock Timebase**)
Frequency resolution	
Internal Sample clock timebase	355 nHz
External Sample clock timebase	**Sample Clock Timebase** / 2^{48}
I and Q phase resolution	0.0055 °
Tuning time	1 ms

Digital Performance

Maximum NCO spur	<-100 dBFS
Decimating filter passband ripple	<0.1 dB [35]
Decimating filter out-of-band suppression	>80 dB [36]

IF Demodulation Performance

Table 16. IF Demodulation Performance

Modulation Configuration[37]	Measurement Type	Value
GSM Physical Layer[38]	Modulation Error Ratio (MER)	62 dB
	Error Vector Magnitude (EVM)	<0.2% RMS
W-CDMA Physical Layer[39]	MER	52 dB

Modulation Configuration[37]	Measurement Type	Value
	EVM	<0.4% RMS
DVB Physical Layer[40]	MER	48 dB
	EVM	<0.4% RMS
20 MSymbols/s, 64 QAM[41]	MER	39 dB
	EVM	<0.8% RMS
26.09 MSymbols/s, 64 QAM[42]	MER	36 dB
	EVM	<1.0% RMS
34.78 MSymbols/s, 64 QAM[43]	MER	32 dB
	EVM	<1.6% RMS

IQ Baseband Demodulation Performance

Table 17. IQ Baseband Demodulation Performance

Modulation Configuration[44]	Measurement Type	Value
GSM physical layer[45]	Modulation Error Ratio (MER)	41 dB
	Error Vector Magnitude (EVM)	<0.8% RMS
W-CDMA Physical Layer[46]	MER	41 dB
	EVM	<0.9% RMS
DVB Physical Layer[47]	MER	40 dB
	EVM	<0.9% RMS
20 MSymbols/s, 64 QAM[48]	MER	33 dB
	EVM	<1.4% RMS

Waveform Acquisition Times

Table 18. Maximum Acquisition Time[49]

Conditions	64 MB	256 MB
Sample rate = 100 MS/s, OSP disabled	0.336 s	1.34 s
Sample rate = 1 MS/s, real mode, OSP enabled	33.6 s	2 min 14 s

Conditions	64 MB	256 MB
Sample rate = 100 kS/s, real mode, OSP enabled	5 min 36 s	22 min 22 s

Figure 6. Decimation Filter Frequency Response (Real Mode), 10 MS/s Sample Rate, Measured

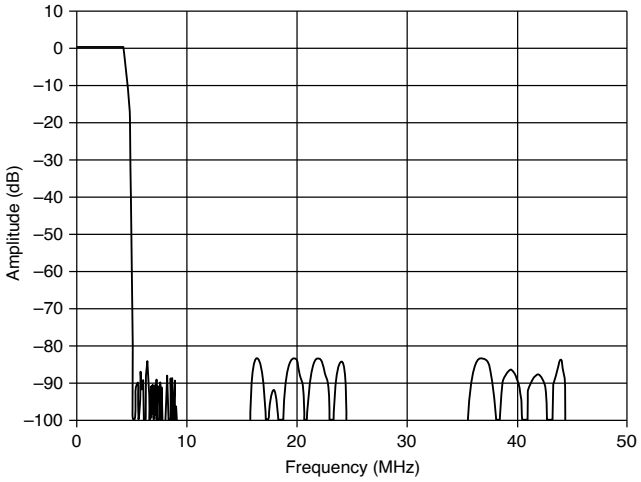


Figure 7. GSM Physical Layer, Measured[50]

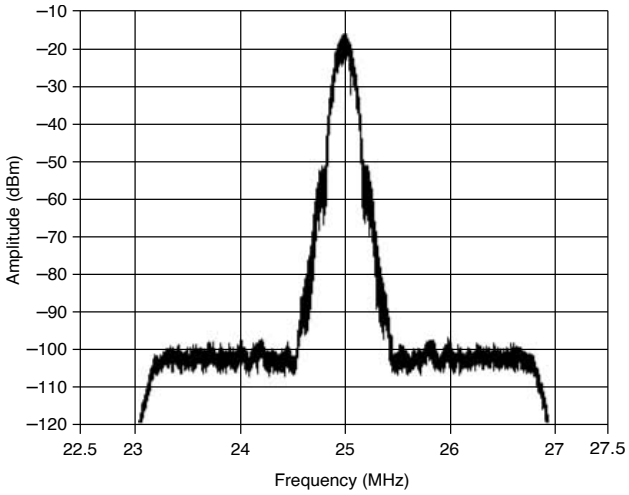


Figure 8. W-CDMA Physical Layer, Measured[51]

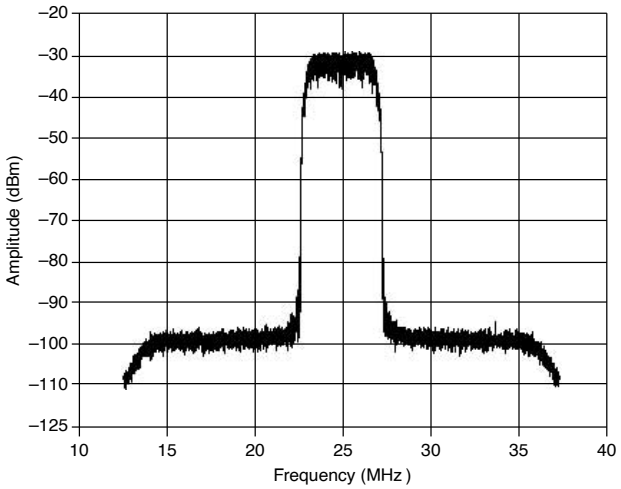


Figure 9. DVB Physical Layer, Measured[52]

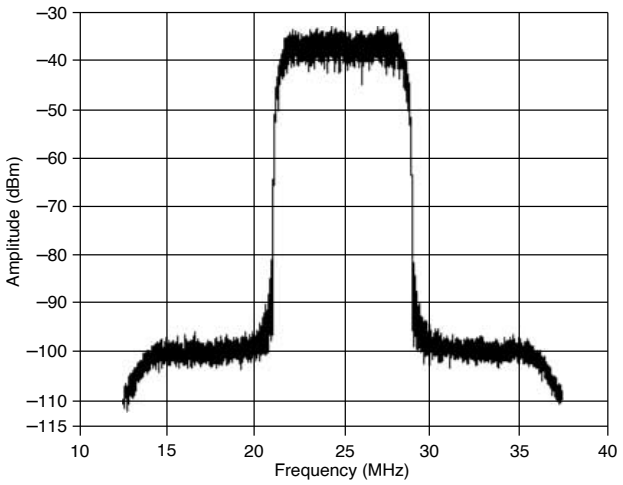
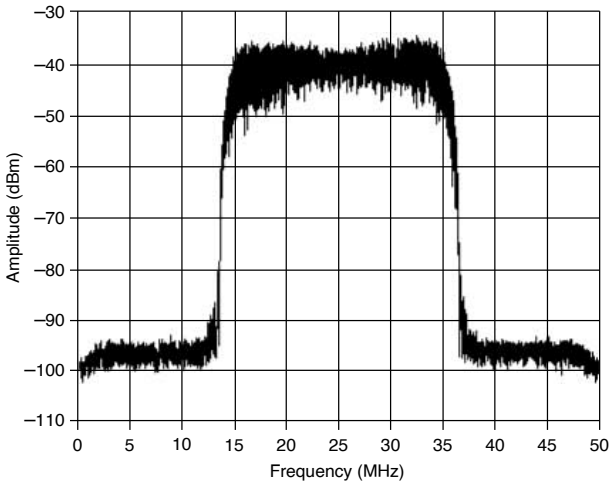


Figure 10. 20 MSymbols/s 64 QAM, Measured[53]



Calibration

External Calibration

External calibration calibrates the VCXO and the voltage reference. All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for gain, offset, frequency response, triggering, and timing adjustment errors for all input ranges.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[54]	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE3.0.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PCI-5142. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PCI-5142 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.

Note InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

Interactive control of the PCI-5142 was first available via InstrumentStudio in NI-SCOPE18.1 and via the NI-SCOPE SFP in NI-SCOPE2.4. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PCI-5142. MAX is included on the driver media.

Synchronization

Synchronization with the NI-TClk API [55]

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PCI-5142 and NI-SCOPE.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

Module-to-module skew, between PCI-5142 modules using NI-TClk [56]	
NI-TClk synchronization without manual adjustment [57]	
Skew, Peak-to-Peak [58]	500 ps
NI-TClk synchronization with manual adjustment [57]	
Skew after manual adjustment	≤5 ps
Sample Clock delay/adjustment resolution	≤5 ps

Power

Current draw	
+3.3 V DC	3.4 A

+5 V DC	2.7 A
+12 V DC	110 mA
-12 V DC	0 A
Total power	26.1 W

Physical

Dimensions	35.5 cm × 2.0 cm × 11.3 cm (14.0 in × 0.8 in × 4.4 in)
Weight	470 g (16.6 oz)

Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2011/65/EU; Restriction of Hazardous Substances (RoHS)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- **中国 RoHS**— NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

PXI-5402 Specifications

2024-01-05

Contents

PXI-5402 Specifications. 3

PXI-5402 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are **Nominal** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted:

- Ambient temperature range of 0 °C to 55 °C
- Analog filter enabled
- Interpolation set to maximum allowed factor for a given sample rate
- Signals terminated with 50 Ω
- Full operating temperature range

Typical specifications are valid under the following conditions unless otherwise noted:

- Ambient temperature range of 15 °C to 35 °C

CH 0

Number of channels	1
Connector type	BNC

Output Voltage

Maximum voltage	±5 V (ACpk + DC)
DAC resolution	14 bits

Amplitude and Offset

Amplitude range[1]	
50 Ω load	5.64 mVpk-pk to 10 Vpk-pk
High-impedance load	11.28 mVpk-pk to 20 Vpk-pk
Amplitude resolution	<0.06% (0.004 dB) of amplitude range
Offset range[2]	
Square waveforms	±50% of amplitude range
All other waveforms	±5 V

Accuracy

AC amplitude accuracy[3]	+2.0% of amplitude +1 mV

	-1.0% of amplitude -1 mV
Offset accuracy[4]	±0.5% of offset ±2 mV±0.5% of amplitude

Output Characteristics

Output impedance	Software-selectable: 50 Ω or 75 Ω
Output enable	Software-selectable: When the output path is disabled, the CH 0 output is terminated to ground with a 1 W resistor with a value equal to the selected output impedance
Maximum output overload	The CH 0 output can be connected to a 50 Ω, ±12 V source without sustaining any damage. No damage occurs if the CH 0 output is shorted to ground indefinitely.
Waveform summing	Outputs of multiple PXI-5402 signal generators can be connected together
Phase adjustment	-180° to +180°
Digital interpolation filter[5]	Software-selectable: Finite Impulse Response (FIR) filter with available interpolation factors of 2 or 4
Analog filter	Software-selectable: 7-pole elliptical filter
Frequency resolution	0.355 µHz

Maximum Frequencies for Common Functions

Maximum frequencies[6]

Sine	20 MHz
Square	20 MHz
Ramp	1 MHz
Triangle	1 MHz
User-defined[7]	20 MHz
Maximum sample rate	
Sine	400 MS/s
Square	400 MS/s
Ramp	100 MS/s
Triangle	100 MS/s
User-defined[7]	400 MS/s
Noise	100 MS/s

Sine Waves

- Spectral characteristics may degrade when offset is applied.
- Spectral characteristics at low amplitudes are limited by a -148 dBm/Hz noise floor.
- Output amplitude of -1 dBFS is used for all spectral specifications.

Passband flatness[8]	±0.4 dB (±5%)

The data presented in the following figures were acquired with the Rohde & Schwarz NRVS Power Meter using the NRV-Z51 Thermal Power Sensor.

Figure 1. Passband Flatness, Expected Voltage 10 Vpk-pk (23.98 dBm)

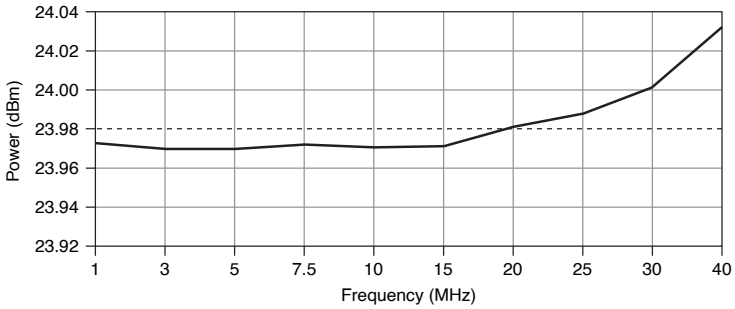
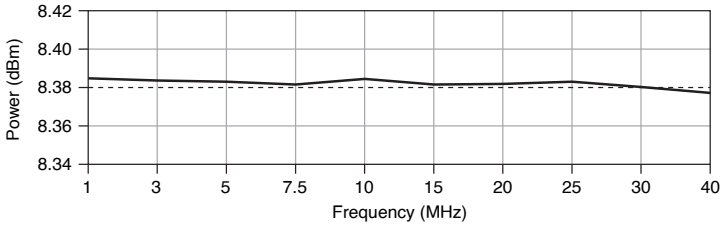


Figure 2. Passband Flatness, Expected Voltage 1.66 Vpk-pk (8.38 dBm)



Spurious-free dynamic range (SFDR)[9] with harmonics[10]	
<10 MHz	50 dB, typical
10 MHz to 20 MHz	45 dB, typical
SFDR[9] without harmonics[11]	70 dB, typical
Total harmonic distortion (THD)[12]	
DC to 1 MHz	
≤1.66 Vpk-pk	–60 dBc, typical
>1.66 Vpk-pk	–58 dBc, typical
1 MHz to 20 MHz	
≤1.66 Vpk-pk	–41 dBc

>1.66 Vpk-pk	–32 dBc
Signal to Noise and Distortion (SINAD)[11]	
DC to 1 MHz	
≤1.66 Vpk-pk	58 dBc
>1.66 Vpk-pk	58 dBc
1 MHz to 20 MHz	
≤1.66 Vpk-pk	41 dBc
>1.66 Vpk-pk	32 dBc
Average noise density	–114 dBm/Hz
Phase noise density[13]	
100 Hz	–100 dBc/Hz
1 kHz	–110 dBc/Hz
10 kHz	–120 dBc/Hz
Jitter (RMS)[14]	<4.0 ps rms

Square Waves

Pulse response	
Rise/fall time	<12 ns, typical
Aberration (undershoot/overshoot)	<5%, typical
Duty cycle[15]	

<10 MHz	20% to 80%
10 MHz to 20 MHz	50%
Jitter (RMS)[16]	
<2 MHz	0.01% of period + 500 ps, typical
≥2 MHz	0.1% of period + 70 ps

User-Defined Waves

Waveform size	16,384 samples

Frequency List Mode

Frequency steps	1 to 58,235 steps
Step duration	1 ms to 21 s

Sample Clock

Source[17]	Onboard VCXO
Frequency accuracy[18]	±25 ppm
Interpolation[19]	1 (off) 2 4

Destinations[20]	SYNC OUT/PFI 0 (BNC front panel connector) PFI 1 (BNC front panel connector) PXI_Trig<0..6> (backplane connector)
Maximum frequency[21]	
SYNC OUT/PFI 0	100 MHz
PFI 1	100 MHz
PXI_Trig<0..6>	20 MHz
Jitter[21]	
SYNC OUT/PFI 0	6 ps rms, typical
PFI 1	12 ps rms, typical
Duty cycle[21]	
SYNC OUT/PFI 0	25% to 65%
PFI 1	25% to 65%

Phase-Locked Loop (PLL) Reference Clock

Sources[22]	REF IN (BNC front panel connector) PXI_CLK10 (backplane connector) None
Frequency accuracy[23]	When using the PLL, the frequency accuracy of the PXI-5402 is solely dependent on the

	frequency accuracy of the PLL Reference Clock source
Lock time	200 ms, maximum 70 ms, typical
Frequency range[24]	5 MHz to 20 MHz, in steps of 1 MHz. The default value is 10 MHz.
Allowed duty cycle range	40% to 60%
Destinations	SYNC OUT/PFI 0 (BNC front panel connector) PFI 1 (BNC front panel connector) PXI_Trig<0..6> (backplane connector)

TClk Synchronization

Intermodule SMC Synchronization Using NI-TClk for Identical Modules

National Instruments TClk synchronization method and the NI-TClk instrument driver are used to align the Sample Clocks on any number of SMC-based modules in a chassis.

- Specifications are valid for any number of PXI modules installed in one PXI-1042 chassis
- All parameters are set to identical values for each SMC-based module
- Sample Clock is set to 100 MS/s, Divide-by-N, and all filters are disabled
- For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support

Skew[25]	500 ps, typical
Average skew after manual adjustment[26]	<10 ps, typical
Sample Clock delay/adjustment resolution	≤10 ps, typical

Note Although you can use NI-TClk to synchronize nonidentical modules, these specifications apply only to synchronizing identical modules.

REF IN

Connector type	BNC
Direction	Input
Input voltage range	
Sine wave	0.63 Vpk-pk to 2.8 Vpk-pk into 50 Ω (0 dBm to +13 dBm)
Square wave	0.2 Vpk-pk to 2.8 Vpk-pk into 50 Ω
Maximum input overload	±10 V (ACpk + DC)
Input impedance	50 Ω
Input coupling	AC

SYNC OUT/PFI 0 and PFI 1

Connector type	BNC (x2)

Direction	Bidirectional
Frequency range	DC to 100 MHz
As an input (trigger)	
Destination	Start Trigger
Maximum input overload	-2 V to +7 V (ACpk + DC)
V_{IH}	2.0 V
V_{IL}	0.8 V
Input impedance	1 kΩ
As an output (event)	
Sources	Sample Clock divided by integer K ($1 \le K \le 4{,}194{,}304$) PLL Reference Clock Exported Start Trigger (Out Start Trigger) SYNC OUT
Output impedance	50 Ω
Maximum output overload	-2 V to +7 V (ACpk + DC)
Minimum V_{OH} [27]	
50 Ω load	1.4 V
High-impedance load	2.9 V

Maximum V_{OL}[27]	
50 Ω load	0.2 V
High-impedance load	0.2 V
Rise/fall time (20% to 80%)[28]	≤2.0 ns

Sync

Sync duty cycle	20% to 80%
Jitter (RMS)[29]	
<2 MHz	0.01% of period + 500 ps, typical
≥2 MHz	0.1% of period + 70 ps

Start Trigger

Sources	SYNC OUT/PFI 0 (BNC front panel connector) PFI 1 (BNC front panel connector) PXI_Trig<0..7> (backplane connector) PXI Star Trigger (backplane connector) Software (use node or function call) Immediate (does not wait for a trigger.) The default is Immediate.
Modes	Single

	Continuous Stepped Burst
Edge detection	Rising Falling Level high Level low
Minimum pulse width	25 ns
Delay from Start Trigger to CH 0 analog output	
Sine waveforms	1,100 ns, typical
Square waveforms	1,100 ns + 0.5% of period, typical
All other waveforms	900 ns
Destinations	SYNC OUT/PFI 0 (BNC front panel connector) PFI 1 (BNC front panel connector) PXI_Trig<0..6> (backplane connector)
Exported trigger delay	65 ns, typical
Exported trigger pulse width	>150 ns

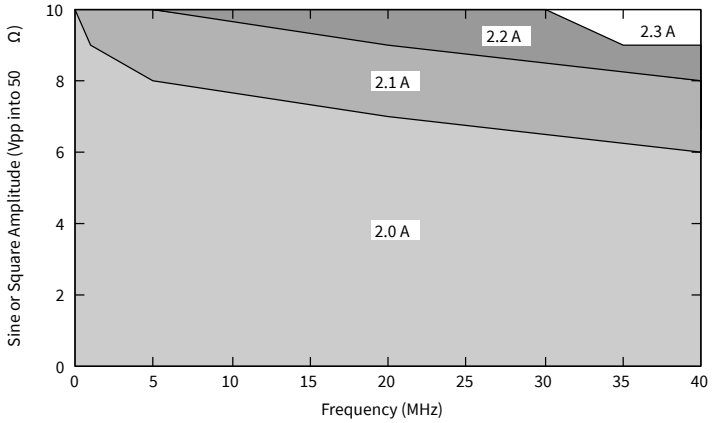
Calibration

Self-calibration	An onboard, 24-bit ADC and precision voltage reference are used to calibrate the gain and offset. Square waveform duty cycle is also calibrated. The self-calibration is initiated by the user through the software and takes approximately 105 seconds to complete.
External calibration[30]	External calibration calibrates the VCXO, voltage reference, self-calibration ADC, flatness, gain, and offset. Appropriate constants are stored in nonvolatile memory.
Calibration interval	Specifications valid within two years of external calibration
Warm-up time	15 minutes

Power

+3.3 VDC	1.4 A
+5 VDC	Refer to the following figure
+12 VDC	0.11 A
-12 VDC	0.01 A
Total power	17.6 W

Figure 3. 5 V Current Versus Frequency and Amplitude



Environment

Maximum altitude	2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 55 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.) 0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.) when installed in a PXI-101x or PXI-1000B chassis
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-25 °C to 85 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Shock	
Operating[31]	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Storage	50 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)
Random vibration	
Operating[31]	5 Hz to 500 Hz, 0.31 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.46 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Physical

Dimensions	3U, one-slot, PXI/cPCI module 21.6 cm × 2.0 cm × 13.0 cm (8.5 in. × 0.8 in. × 5.1 in.)

Weight	351 g (12.4 oz)

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For safety certifications, refer to the product label or the Product Certifications and Declarations section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the Product Certifications and Declarations section.

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the **Engineering a Healthy Planet** web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

EU and UK Customers

- **Waste Electrical and Electronic Equipment (WEEE)**—At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

- **中国 RoHS**— NI 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 NI 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

PXIe-5163 Specifications

2024-01-05

Contents

PXIe-5163 Specifications. 3

PXIe-5163 Specifications

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- **Measured** specifications describe the measured performance of a representative model.

Specifications are **Nominal** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges, bandwidths, and bandwidth-limiting filters
- Sample rate set to 1 GS/s
- Onboard sample clock locked to onboard reference clock
- 15-minute warm-up time at ambient temperature

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 50 °C
- Calibration cycle maintained
- Chassis configured:[1]
  - PXI Express chassis fan speed set to HIGH
  - Foam fan filters removed if present
  - Empty slots contain PXI chassis slot blockers and filler panels
- External calibration performed at 23 °C ± 3 °C
- Within ±5 °C of temperature at last self-calibration as reported by onboard temperature sensor

Typical specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 50 °C

Vertical

Analog Input

Number of channels	Two (simultaneously sampled)
Input type	Referenced single-ended
Connectors	BNC, ground referenced

Impedance and Coupling

Input impedance	50 Ω ±1.25%, typical 1 MΩ ±0.5%, typical
Input capacitance (1 MΩ)	20.2 pF ±2.5 pF, typical

Input coupling	AC DC

Figure 1. 50 Ω Voltage Standing Wave Ratio (VSWR)

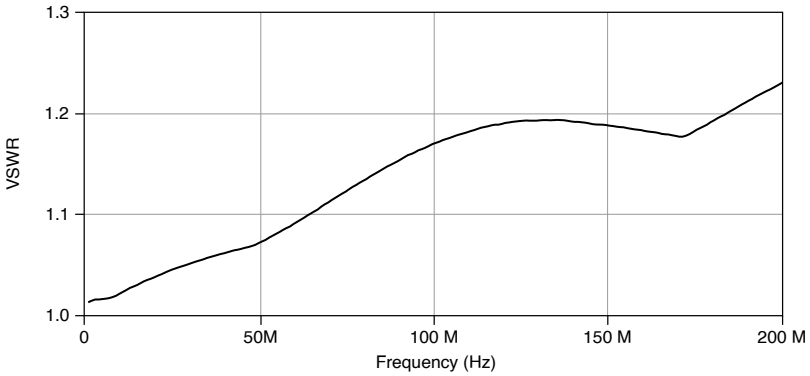
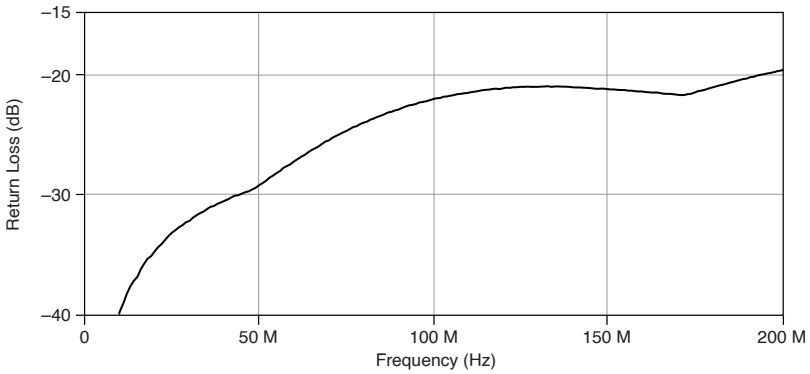


Figure 1. 50 Ω Input Return Loss



Voltage Levels

50 Ω FS input range (V_{pk-pk})	0.25 V 0.5 V 1 V 2.5 V 5 V

Table 1. 1 MΩ FS Input Range and Vertical Offset Range

Input Range (V_{pk-pk})	Vertical Offset Range[2] (V)
0.25 V	±5
0.5 V	±5
1 V	±5
2.5 V	±10 or ±248.75
5 V	±10 or ±247.5
10 V	±10 or ±245
25 V	±50 or ±237.5
50 V	±50 or ±225
100 V	±50 or ±200
Maximum input overload	
50 Ω	|Peaks| ≤5 V
1 MΩ [3]	250 V RMS

Notice Signals exceeding the maximum input overload may cause damage to the device.

Accuracy

Resolution	14 bits
DC accuracy[4], [5]	
50 Ω	±[(0.5% × |**Reading**|) + (0.2% of FS)], warranted
1 MΩ	±[(0.65% × |**Reading** - **Vertical Offset**|) + (0.4% × |**Vertical Offset**|) + (0.2% of FS) + 0.15 mV], warranted

DC drift[6]	±0.0013 dB per °C at 50 kHz
AC amplitude accuracy[4]	±0.225 dB at 50 kHz, warranted

Crosstalk Crosstalk is measured on one channel with a test signal applied to the other channel and the same range setting on both channels.

Table 2. 50 Ω Crosstalk

Frequency	Level
1 MHz	-100 dB
10 MHz	-100 dB
100 MHz	-85 dB
200 MHz	-75 dB

Table 3. 1 MΩ Crosstalk

Frequency	Level	
	0.25 V to 10 V (V_{pk-pk})	25 V to 100 V (V_{pk-pk})
1 MHz	-85 dB	-70 dB
10 MHz	-85 dB	-70 dB
100 MHz	-75 dB	-55 dB
200 MHz	-70 dB	-50 dB

Bandwidth and Transient Response

Bandwidth (-3 dB)[7],[8]	200 MHz, warranted
Bandwidth-limiting filters[7],[8]	
Lowpass filters	20 MHz 30 MHz

	150 MHz
Highpass filters	90 Hz 450 Hz
Passband amplitude flatness (at <150 MHz)[7],[8]	
50 Ω	±0.5 dB, warranted
1 MΩ	±0.7 dB, typical
AC-coupling cutoff (-3 dB)	
50 Ω [9]	40 kHz
1 MΩ [8]	7.5 Hz
Rise/fall time[10]	2 ns

Figure 1. 50 Ω Full Bandwidth Frequency Response, 1 $V_{pk\text{-}pk}$, Measured

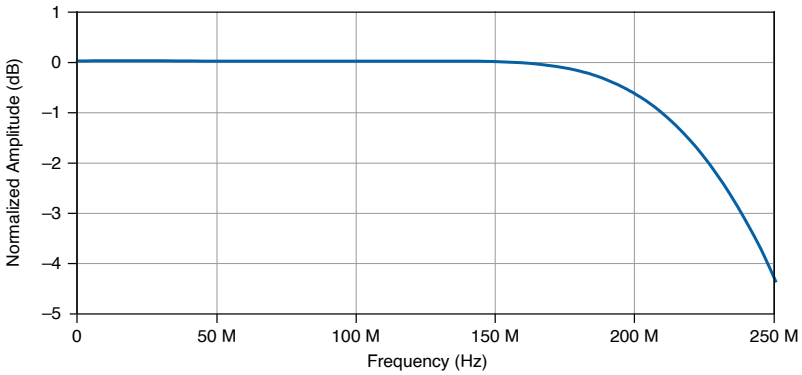


Figure 1. 50 Ω Full Bandwidth Frequency Response Zoomed, 1 V_{pk-pk}, Measured

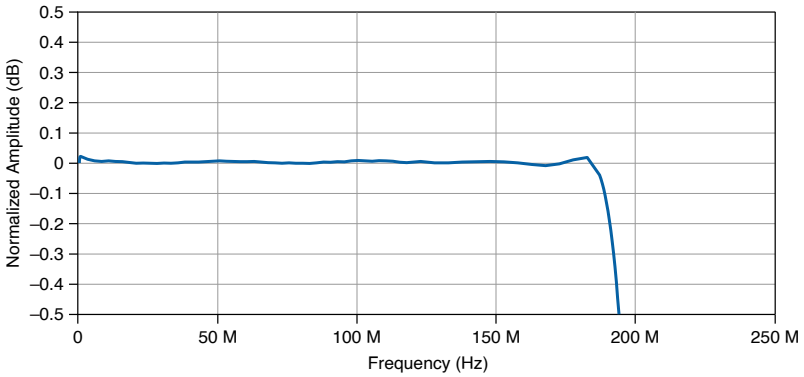


Figure 1. 50 Ω 150 MHz Bandwidth Frequency Response, 1 V_{pk-pk}, Measured

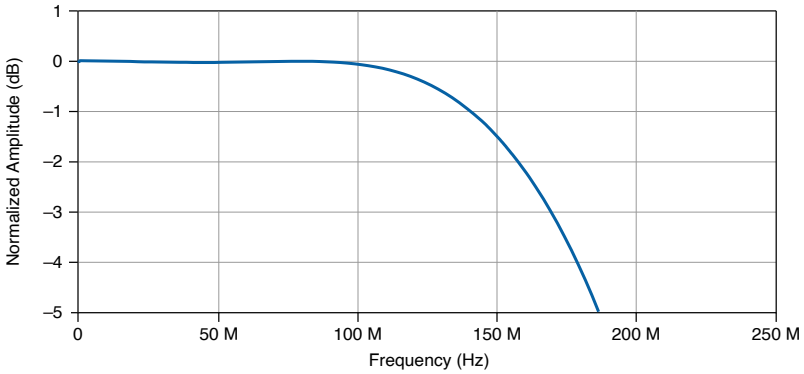


Figure 1. 1 MΩ Full Bandwidth Frequency Response, 1 V_{pk-pk}, Measured

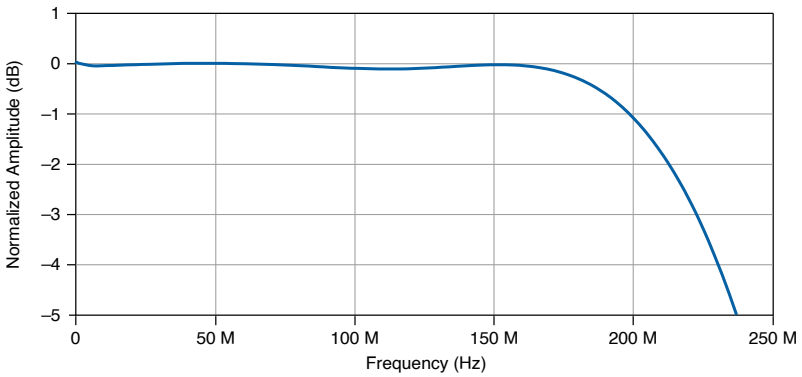


Figure 1. 1 MΩ Full Bandwidth Frequency Response Zoomed, 1 V_{pk-pk}, Measured

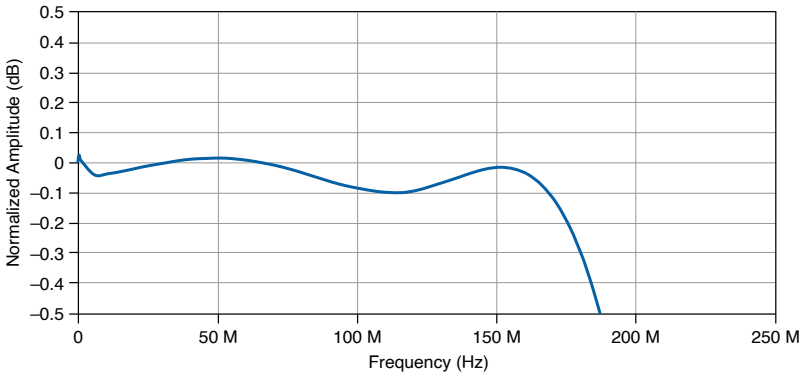
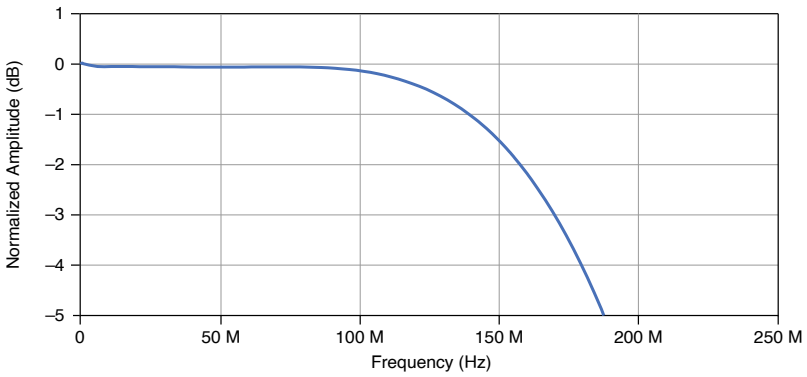


Figure 1. 1 MΩ 150 MHz Bandwidth Frequency Response, 1 V_{pk-pk}, Measured



Spectral Characteristics

50 Ω Spectral Characteristics Excludes ADC interleaving spurs. 1

Table 4. Spurious-Free Dynamic Range (SFDR)[11]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth (dBc)
0.25 V	-70
0.5 V	-73
1 V	-73
2.5 V	-73
5 V	-70

Table 5. Total Harmonic Distortion (THD)[12]

Input Range (V_{pk-pk})	<50 MHz, Full Bandwidth (dBc)	≥50 MHz to ≤100 MHz, Full Bandwidth (dBc)
0.25 V	-73	-69
0.5 V	-73	-72
1 V	-72	-70
2.5 V	-72	-68
5 V	-72	-69

Table 6. Effective Number of Bits (ENOB)[11]

Input Range (V_{pk-pk})	<100 MHz, Full Bandwidth	<100 MHz, 150 MHz Filter
0.25 V	10.5	10.7
0.5 V	10.7	10.9
1 V	10.7	11.0
2.5 V	10.9	11.1
5 V	10.8	11.0

Figure 1. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk} Input Range, 150 MHz Filter, 9.9 MHz Input Tone at -1 dBFS, Measured

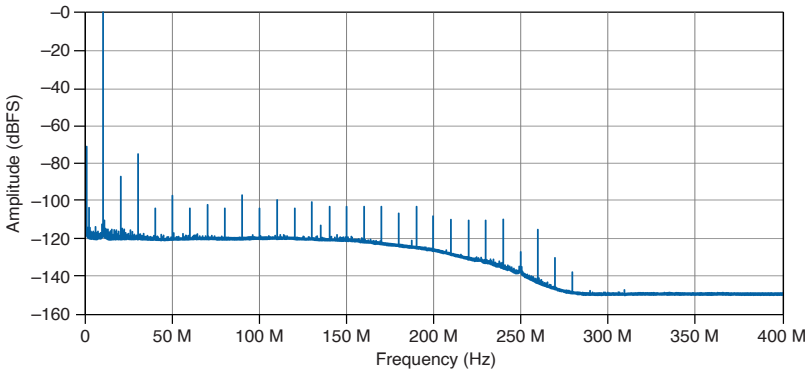


Figure 1. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Measured

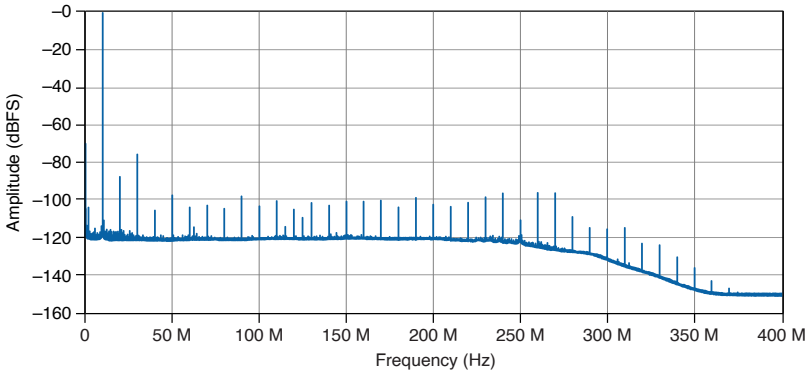
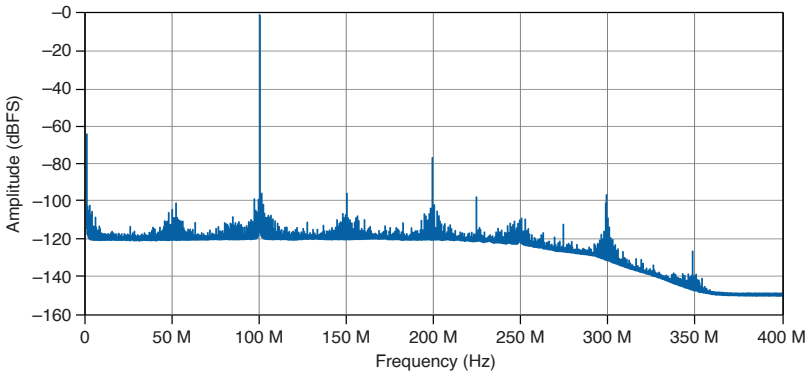


Figure 1. 50 Ω Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 99.9 MHz Input Tone at -1 dBFS, Measured



1 MΩ Spectral Characteristics 1 , Verified using a 50 Ω source and 50 Ω feed-through terminator.

Figure 1. 1 MΩ Single-Tone Spectrum, 1 V_{pk-pk} Input Range, 150 MHz Filter, 9.9 MHz Input Tone at -1 dBFS, Measured

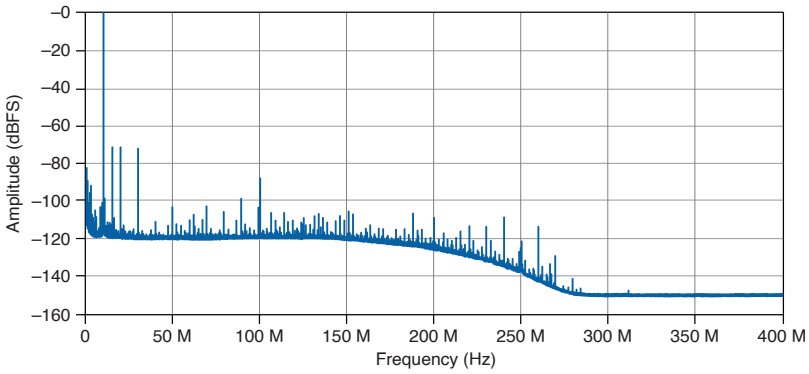
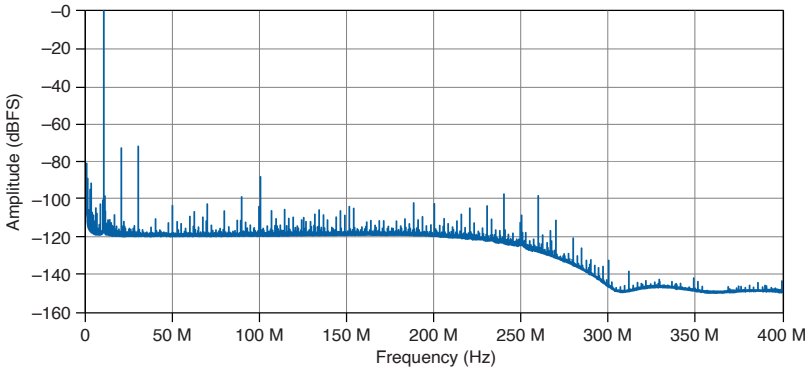


Figure 1. 1 MΩ Single-Tone Spectrum, 1 V_{pk-pk} Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Measured



Noise[13]

50 Ω RMS Noise

Input Range (V_{pk-pk})	RMS Noise (% of FS)	
	Full Bandwidth, Warranted	150 MHz Filter, Typical
0.25 V	0.045	0.018
0.5 V	0.040	0.018
1 V	0.035	0.017
2.5 V	0.030	0.017
5 V	0.030	0.014

Figure 1. 50 Ω Channel 0 Average Noise Density, 1 V_{pk-pk} Range, Measured

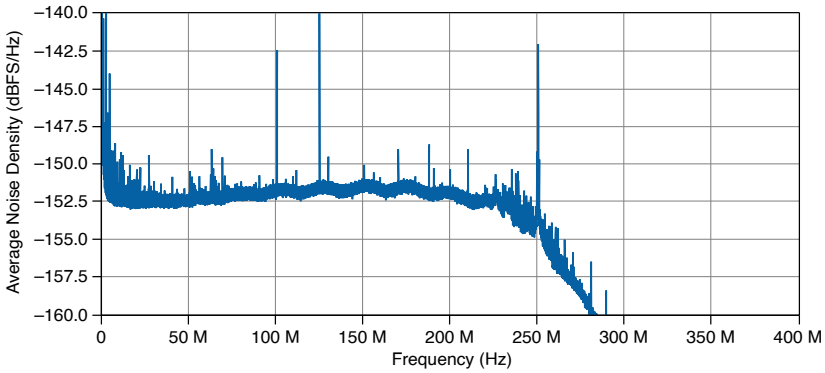
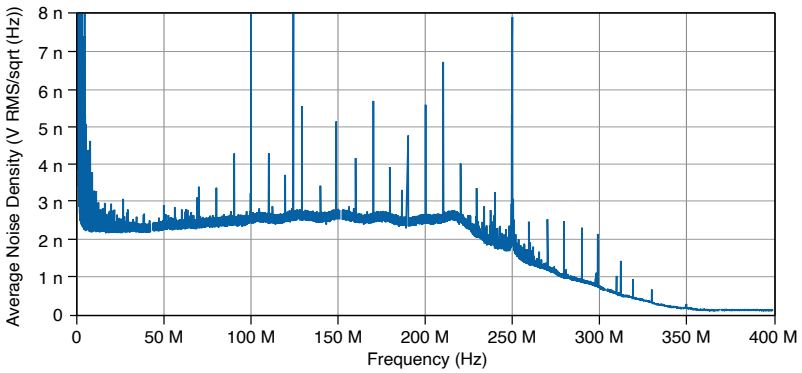


Figure 1. 50 Ω Channel 0 Average Noise Density, 0.25 V_{pk-pk} Range, Measured



1 MΩ RMS Noise

Input Range (V_{pk-pk})	RMS Noise (% of FS)	
	Full Bandwidth, Warranted	150 MHz Filter, Typical
0.25 V	0.110	0.070
0.5 V	0.060	0.050
1 V	0.050	0.030
2.5 V	0.100	0.055
5 V	0.060	0.045
10 V	0.050	0.030
25 V	0.080	0.050

Input Range (V_{pk-pk})	RMS Noise (% of FS)	
	Full Bandwidth, Warranted	150 MHz Filter, Typical
50 V	0.060	0.040
100 V	0.050	0.030

Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCTCXO)
External	CLK IN (front panel SMB connector) PXIe-DSTAR_A (backplane connector)
Sample rate range, real-time[14]	15.259 kS/s to 1 GS/s
Timebase frequency	1.0 GHz
Timebase accuracy	
Phase-locked to onboard clock	±5 ppm, warranted
Phase-locked to external clock	Equal to the external clock accuracy
Sample clock jitter[15]	500 fs RMS

Phase-Locked Loop (PLL) Reference Clock

Sources	
Internal	Onboard clock (internal VCTCXO)

	PXI_CLK10 (backplane connector)
External (10 MHz)	CLK IN (front panel SMB connector) AUX 0 CLK IN (front panel MHDMR connector)
Duty cycle tolerance	45% to 55%, typical

External Sample Clock

Source	CLK IN (front panel SMB connector)
Impedance	50 Ω
Coupling	AC
Frequency	1.0 GHz
Input voltage range, when configured as a sample clock	632 mV_{pk-pk} to 5 V_{pk-pk} (0 dBm to 18 dBm), typical
Maximum input overload, when configured as a sample clock	6 V_{pk-pk}
Duty cycle tolerance	45% to 55%, typical

External Reference Clock In

Sources	CLK IN (front panel SMB connector) AUX 0 CLK IN (front panel MHDMR connector)

Impedance	50 Ω
Coupling	AC
Frequency[16]	10 MHz
Input voltage range, when configured as a reference clock	623 mV_{pk-pk} to 5 V_{pk-pk} (0 dBm to 18 dBm), typical
Maximum input overload, when configured as a reference clock	6 V_{pk-pk}

Reference Clock Out

Source	PXI_CLK10 (backplane connector)
Destination	AUX 0 CLK OUT (front panel MHDMR connector)
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	±12 mA

Trigger

Supported triggers	Reference (stop) trigger Reference (arm) trigger Start trigger

	Advance trigger
Trigger types	Edge Window Hysteresis Digital Immediate Software
Trigger sources	CH 0 CH 1 SMB PFI 0 AUX 0 PFI <0..7> PXI_Trig <0..6> Software
Trigger delay	from 0 ns to 2.25×10^{15} ns ($(2^{51} - 1) \times$ **Sample Clock Period** ns)
Dead time	496 ns
Hold off	From dead time to 1.84×10^{19} ns ($(2^{64} - 1) \times$ **Sample Clock Period** ns)

Analog Trigger

Sources	CH 0 CH 1
Time resolution	
Interpolator enabled	**Sample Clock Period** / 1024 = 0.977 ps
Interpolator disabled	Sample clock period (1 ns)
Trigger filters	
Low Frequency (LF) Reject	100 kHz
High Frequency (HF) Reject	100 kHz
Trigger accuracy[17]	0.5% of FS
Trigger jitter[17]	15 ps RMS
Minimum threshold duration[18]	Sample clock period

Digital Trigger

Sources	PFI 0 (front panel SMB connector) AUX 0 PFI <0..7> (front panel MHDMR connector) PXI_Trig <0..6> (backplane connector)
Time resolution	8 ns

Programmable Function Interface

Connectors	AUX 0 PFI <0..7> (front panel MHDMR connector) PFI 0 (front panel SMB connector)
Direction	Bidirectional per channel
As an input (trigger)	
Destination	Start trigger (acquisition arm) Reference (stop) trigger Arm reference trigger Advance trigger
Input impedance	49.9 kΩ
V_{IH}	2 V, typical
V_{IL}	0.8 V, typical
Recommended input range	3.3 V
Maximum input overload	0 to 3.3 V (5 V tolerant)
Maximum frequency	50 MHz
Minimum pulse width	10 ns
As an output (event)	
Sources	Ready for Start

	Start trigger (acquisition arm) Ready for Reference Reference (stop) trigger End of Record Ready for Advance Advance trigger Done (end of acquisition) Probe compensation[19]
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	12 mA
Maximum frequency	50 MHz
Minimum pulse width	10 ns

AUX 0 Connector Specifications

Connector	MHDMR
Voltage output	3.3 V ±10%
Maximum current drive on +3.3 V	200 mA

Output impedance on +3.3 V	<1 Ω

Waveform Specifications

Onboard memory size[20]	512 MB
Minimum record length	1 sample
Number of pretrigger samples	Zero up to (**Record Length** - 1)
Number of posttrigger samples	Zero up to **Record Length**
Maximum number of records in onboard memory[21]	1,398,101 for 512 MB

Table 10. Examples of Allocated Onboard Memory Per Record (512 MB Onboard Memory)

Channels	Bytes per Sample	Max Records per Channel	Record Length	Allocated Onboard Memory per Record
1	2	1,398,101	1	384
1	2	223,696	1,000	2,400
1	2	26,379	10,000	20,352
1	2	1	268,435,265	536,870,912
2	2	1,398,101	1	384
2	2	121,574	1,000	4,416
2	2	13,283	10,000	33,216
2	2	1	134,217,633	536,870,912

Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, which is available at ni.com/manuals.

Calibration

External Calibration

External calibration yields the following benefits:

- Corrects for gain and offset errors of the onboard references used in self-calibration.
- Adjusts timebase accuracy.
- Compensates the 1 MΩ ranges.
- Corrects the frequency response for all ranges.

All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for the following aspects:

- Gain
- Offset
- Interleaving spurs
- Intermodule synchronization errors

Refer to the **NI High-Speed Digitizers Help** for information about when to self-calibrate the device.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[22]	15 minutes

Software

Driver Software

Driver support for this device was first available in NI-SCOPE18.7.

NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the PXIe-5163. NI-SCOPE provides application programming interfaces for many development environments.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can use InstrumentStudio to monitor, control, and record measurements from the PXIe-5163.

InstrumentStudio is an application that allows you to perform interactive measurements on several different NI device types in a single application.

Interactive control of the PXIe-5163 was first available via InstrumentStudio in NI-SCOPE18.7. InstrumentStudio is included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5163. MAX is included on the driver media.

Synchronization

Channel-to-channel skew, between the channels of a PXIe-5163	
50 Ω	<100 ps
1 MΩ	<150 ps

Note The channels of a PXIe-5163 are automatically synchronized when they are in the same NI-SCOPE session.

Synchronization with the NI-TClk API [23]

NI-TClk is an API that enables system synchronization of supported PXI modules in one or more PXI chassis, which you can use with the PXIe-5163 and NI-SCOPE.

NI-TClk uses a shared Reference Clock and triggers to align the Sample Clocks of PXI modules and synchronize the distribution and reception of triggers. These signals are routed through the PXI chassis backplane without external cable connections between PXI modules in the same chassis.

Module-to-module skew, between PXIe-5163 modules using NI-TClk [24]	
NI-TClk synchronization without manual adjustment [25]	
Skew, peak-to-peak [26]	300 ps, typical
NI-TClk synchronization with manual adjustment [25]	
Skew, average	≤10 ps
Sample Clock delay/adjustment resolution	3.5 ps

Power Requirements

Current draw

+3.3 V DC	1.97 A
+12 V DC	1.63 A
Power draw	
+3.3 V DC	6.5 W
+12 V DC	19.5 W
Total	26 W

Physical

Dimensions	3U, one-slot, PXI Express Gen 2 x8 module 21.26 cm × 12.88 cm × 2.0 cm (8.37 in. × 5.07 in. × 0.787 in.)
Weight	460 g (16.2 oz)

Bus Interface

Form factor	PXI Express (x8 Gen 2)
Slot compatibility	PXI Express or hybrid

Environmental Characteristics

Temperature	
Operating	0 °C to 50 °C

Storage	-40 °C to 71 °C
Humidity	
Operating	10% to 90%, noncondensing
Storage	5% to 95%, noncondensing
Pollution Degree	2
Maximum altitude	4,600 m (570 mbar) (at 25 °C ambient temperature)
Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit ni.com/product-certifications, search by model number, and click the appropriate link.

PXIe-4141 Specifications

2024-01-05

Contents

PXIe-4141 Specifications. 3

PXIe-4141 Specifications

These specifications apply to the PXIe-4141.

Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- **Typical** specifications describe the performance met by a majority of models.
- **Nominal** specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are **Warranted** unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature[1] of 23 °C ± 5 °C
- Calibration interval of 1 year
- 30 minutes warm-up time
- Self-calibration performed within the last 24 hours
- niDCPower Aperture Time property or NIDCPOWER_ATTR_APERTURE_TIME attribute set to 2 power-line cycles (PLC)
- Fans set to the highest setting if the PXI Express chassis has multiple fan speed settings

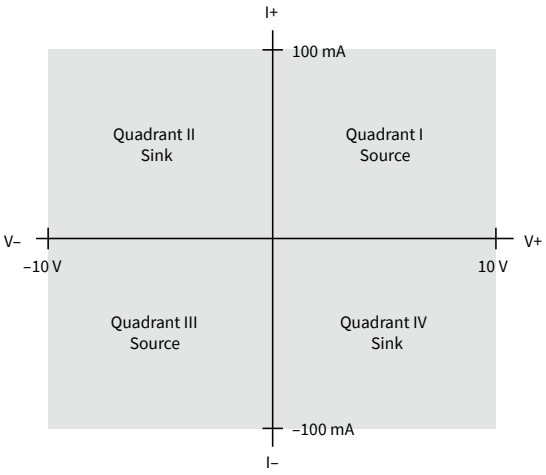
Device Capabilities

The following table and figure illustrate the voltage and the current source and sink ranges of the PXIe-4141.

Table 1. Current Source and Sink Ranges

Channels	DC Voltage Ranges	DC Current Source and Sink Ranges
0 through 3	±10 V	▪ 10 µA ▪ 100 µA ▪ 1 mA ▪ 10 mA ▪ 100 mA

Figure 1. Quadrant Diagram, All Channels



SMU Specifications

Voltage Programming and Measurement Accuracy/ Resolution

Table 2. Voltage Programming and Measurement Accuracy/Resolution

Range	Resolution and noise (0.1 Hz to 10 Hz)	Accuracy (23 °C ± 5 °C) ± (% of voltage + offset) [2]		Tempco ± (% of voltage + offset)/°C, 0 °C to 55 °C
		T_{cal} ± 5 °C	T_{cal} ± 1 °C	
10 V	10 µV	0.015% + 600 µV	0.013% + 150 µV	0.0005% + 1 µV

Related tasks:

- Calculating SMU Resolution

Related reference:

- Additional Specifications

Current

Table 3. Current Programming and Measurement Accuracy/Resolution

Range	Resolution and noise (0.1 Hz to 10 Hz)	Accuracy (23 °C ± 5 °C) ± (% of current + offset)		Tempco ± (% of current + offset)/°C, 0 °C to 55 °C
		T_{cal} ± 5 °C	T_{cal} ± 1 °C	
10 µA	10 pA	0.03% + 1.5 nA	0.03% + 300 pA	0.002% + 10 pA
100 µA	100 pA	0.03% + 15 nA	0.03% + 3.0 nA	0.002% + 100 pA
1 mA	1 nA	0.03% + 150 nA	0.03% + 30 nA	0.002% + 1.0 nA
10 mA	10 nA	0.03% + 1.5 µA	0.03% + 300 nA	0.002% + 10 nA
100 mA	100 nA	0.03% + 15 µA	0.03% + 3.0 µA	0.002% + 100 nA

Related tasks:

- Calculating SMU Resolution

Related reference:

- Additional Specifications

Output Resistance Programming Accuracy/Resolution, Typical

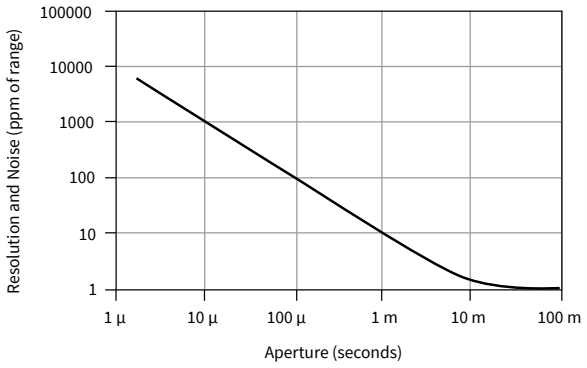
Table 4. Output Resistance Programming Accuracy/Resolution, Typical

Current limit range	Programmable resistance range	Resolution	Accuracy ± (% of resistance setting), T_{cal} ± 5 °C
10 µA	± 100 kΩ	1 Ω	0.04% + 510 mΩ
100 µA	± 10 kΩ	100 mΩ	0.04% + 60 mΩ
1 mA	± 1 kΩ	10 mΩ	0.04% + 15 mΩ
10 mA	± 100 Ω	1 mΩ	0.04% + 10 mΩ
100 mA	± 10 Ω	100 µΩ	0.04% + 10 mΩ

Calculating SMU Resolution

Refer to the following figure as you complete the following steps to derive a resolution in absolute units:

Figure 1. Noise and Resolution versus Measurement Aperture, Typical



1. Select a voltage or current range.
2. For a given aperture time, find the corresponding resolution.
3. To convert resolution from ppm of range to absolute units, multiply resolution in ppm of range by the selected range.

Example of Calculating SMU Resolution

The PXIe-4141 has a resolution of 100 ppm when set to a 100 µs aperture time. In the 10 V range, resolution can be calculated by multiplying 10 V by 100 ppm, as shown in the following equation:

$10\ V * 100\ ppm = 10\ V * 100 * 1\times10^{-6} = 1\ mV$

Likewise, in the 100 mA range, resolution can be calculated by multiplying 100 mA by 100 ppm, as shown in the following equation:

$100\ mA * 100\ ppm = 100\ mA * 100 * 1\times10^{-6} = 10\ \mu A$

Additional Specifications

Settling time[3]	<100 µs to settle to 0.1% of voltage step, device configured for fast transient response, typical
Transient response	<100 µs to recover within ±20 mV after a load current change from 10% to 90% of range, device configured for fast transient response, typical
Wideband source noise[4]	1.5 mV RMS, typical <20 $mV_{pk\text{-}pk}$, typical
Cable guard output impedance	10 kΩ, typical
Remote sense	
Voltage	Add 0.1% of LO lead drop to voltage accuracy specification
Current	Add 0.02% of range per volt of total HI and LO lead drop to current accuracy specification

Maximum lead drop	Up to 1 V drop per lead
Load regulation	
Voltage	10 µV at connector pins per mA of output load when using local sense, typical
Current	20 pA + (10 ppm of range per volt of output change) when using local sense, typical
Isolation voltage, channel-to-earth ground	60 VDC, CAT I, verified by dielectric withstand test, 5 s, continuous, characteristic
Absolute maximum voltage between any terminal and LO	20 VDC, continuous

The following figures illustrate the effect of the transient response setting on the step response of the PXIe-4141 for different loads.

Figure 1. 1 mA Range No Load Step Response, Typical

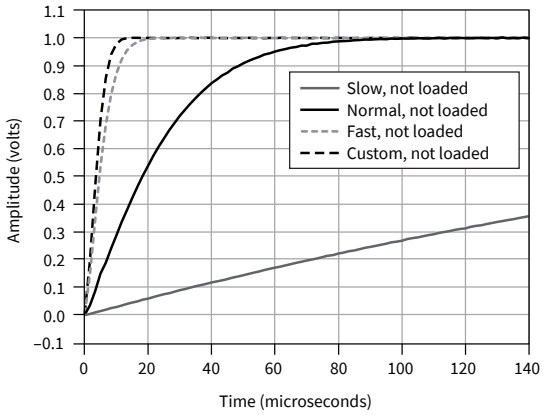
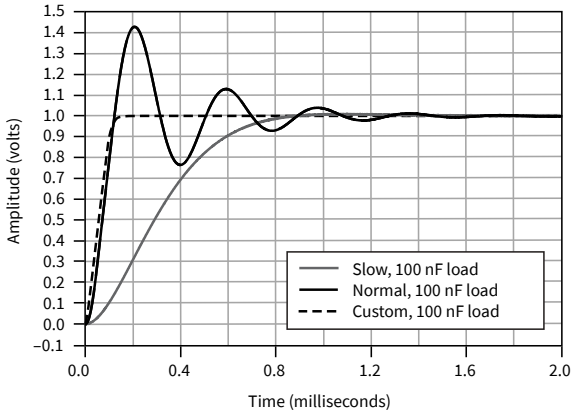


Figure 1. 1 mA Range, 100 nF Load Step Response, Typical



Related reference:

- Voltage Programming and Measurement Accuracy/Resolution
- Current

Supplemental Specifications

Measurement and Update Timing

Available sample rates[5]	(600 kS/s)/N

where

- N = 6, 7, 8, … 2^{20}
- S is samples

Sample rate accuracy	±50 ppm
Maximum measure rate to host[6]	600,000 S/s per channel, continuous
Maximum source update rate[7]	
Sequence length <300 steps per iteration	100,000 updates/s per channel

Sequence length ≥300 steps per iteration	100,000 updates/s per board
Input trigger to	
Source event delay	5 µs
Source event jitter	1.7 µs
Measure event jitter	1.7 µs

Triggers

Input triggers	
Types	Start Source Sequence Advance Measure
Sources (PXI trigger lines 0 to 7)[]	
Polarity	Active high (not configurable)
Minimum pulse width	100 ns
Destinations[9] **(PXI trigger lines 0 to 7)**[]	
Polarity	Active high (not configurable)
Minimum pulse width	200 ns
Output triggers (events)	
Types	Source Complete

	Sequence Iteration Complete Sequence Engine Done Measure Complete
Destinations (PXI trigger lines 0 to 7)[]	
Polarity	Active high (not configurable)
Pulse width	230 ns

Calibration Interval

Recommended calibration interval	1 year

Physical

Dimensions	3U, one-slot, PXI Express/CompactPCI Express module 2.0 cm × 13.0 cm × 21.6 cm (0.8 in. × 5.1 in. × 8.5 in.)
Weight	
20 W	425 g (14.99 oz)
40 W	428 g (15.1 oz)
Front panel connectors	25-position D-SUB, male

Power Requirement

PXIe-4141 (40W)	3.0 A from the 3.3 V rail and 6.0 A from the 12 V rail
PXIe-4141 (20W)	2.5 A from the 3.3 V rail and 2.7 A from the 12 V rail

Environmental Characteristics

Temperature	
Operating	0 °C to 55 °C
Storage	
Humidity	
Operating	10% to 70%, noncondensing. Derate 1.3% per °C above 40 °C.
Storage	5% to 95%, noncondensing.
Pollution Degree	2
Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Shock and Vibration	
Operating vibration	5 Hz to 500 Hz, 0.3 g RMS
Non-operating vibration	5 Hz to 500 Hz, 2.4 g RMS
Operating shock	30 g, half-sine, 11 ms pulse