



Master Seminar (EVA) on Fabrication and Test of Semiconductors

Report on MSE EVA Semiconductors '23

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The Seminar

The Seminar on Test and Fabrication of Semiconductors is part of the Master of Science in Engineering MSE in Electrical Engineering. The aim is to provide interested students insights into the design, fabrication, and testing of semiconductor devices.

The sensor device: The heat transfer between a heating element and nearby temperature sensitive pn-junctions (diodes) depends on the air flow. Thus, sensing the temperature change on the pn-junctions leads to information about the direction and volume of the air flow.

The pn-junctions used as sensing element are built as p⁺nn⁻ junctions. The epitaxial silicon substrate, n-layer on n⁻substrate, is doped by implantation of bor ions (courtesy of Institut für Ionenstrahlphysik und Materialforschung Helmholtz-Zentrum Dresden) to obtain a shallow p⁺-layer.

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Figure 1: Sensor Device

The heating element is based on microstructured meander resistors made of platinum on an insulating aluminum-oxide layer.

Design for Test: The sensor is controlled by additional electronic circuits. The overall system and its subcomponents are designed and prepared for testability. In the process, students will be familiarized with



Figure 2: PXI Test Equipment, Reference: NI, accessed 7.3.2023 <https://www.ni.com/de-ch/shop/pxi.html>.

test ability. In the process, students will be familiarized with test coverage, logic and fault simulation, Built-in self-test, scan test, analog test methods, etc. Design and simulation will be done with state-of-the-art CAD tools with respect to Application Specific Integrated Circuit (ASIC) Implementation. We synthesize a digital part described in VHDL, which we place and route (P&R). After each development step, we simulate the digital circuit and create test patterns with an ATPG tool. However, since the fabrication of a complex ASIC is not possible in such a short time and with the available equipment, the digital part of the circuit is fabricated as Field Programmable Gate Array (FPGA) and the analog part in the form of discrete components.

Fabrication under cleanroom conditions: The tiny dimensions of semiconductor and microtechnology devices require special manufacturing conditions. Very low particle concentration in the and controlled conditions of the air are essential for successful manufacturing. Students have the unique chance to perform wafer processing by themselves. This includes wet chemical etching, photolithography, cleaning, and inspection.

Minimal feature size of 30 μ m with a tolerance below ±5 μ m are realized to obtain a high heating power density. Photolithography and lift-off techniques allow to transfer these patterns into platinum.

The devices are completed with wet chemically patterned Aluminum pads on top.

Assembly: Singulation into devices by wafer dicing is the initial step in the packaging. The devices are mounted on printed circuit boards using a die-bonder and insulating adhesive. Gold wire bonding is used to electrically connect the pads the devices with the respective areas on the Printed Circuit Board (PCB).

Testing:

After fabrication, the circuits are verified with the previously prepared test programs. On the one hand, the test case of a production test is executed, and, on the other hand, the verification of individual components is carried out and compared with the simulation results.

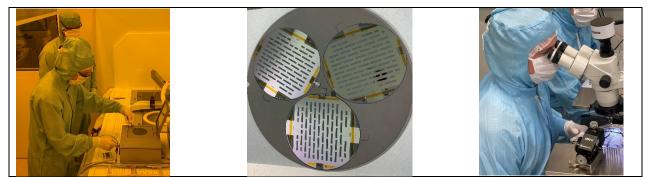


Figure 3: photolithography process to obtain micropatterns on substrates performed by students (left), three silicon wafers mounted on chuck for dielectrica deposition (middle), and studends performing wafer level inspection of device performance (right).

Results: The students successfully completed the fabrication, the assembly and the testing of the air flow sensor device within seven days of practical training. Together with the blended learning sessions, this seminar provided highly valuable insights for motivated students.

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OST

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