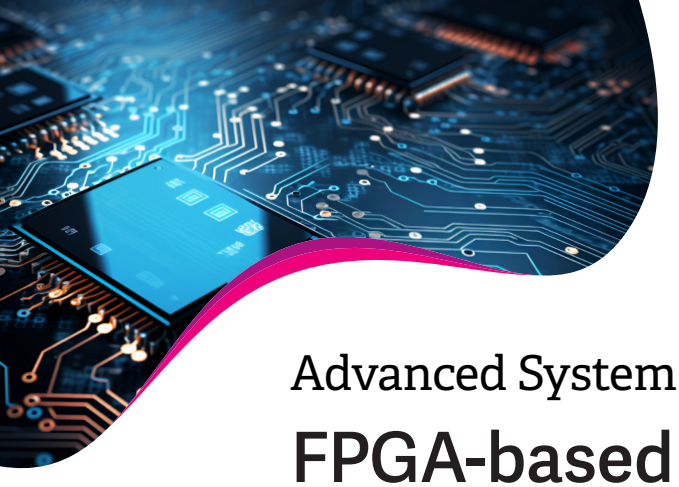

OST
Eastern Switzerland
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Advanced System Technologies

FPGA-based Time-to-Digital Converters

High-precision time measurements in the picosecond range are essential in various industrial and scientific applications. Applications range from Time-of-Flight (ToF) in LiDAR systems to Fluorescence Lifetime Imaging Microscopy (FLIM). The central element of such time measurements is the time-to-digital converter (TDC), which is able to capture the time difference between a start signal and one or more stop signals and convert it into a digital value.

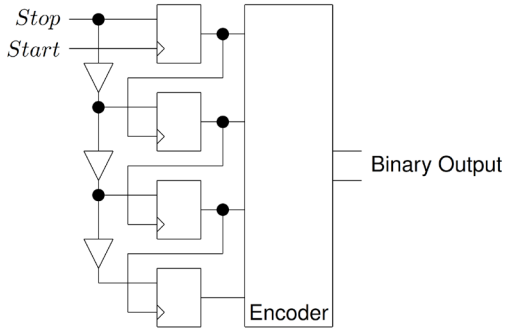

Figure 1: Structure of a Tapped-Delay-Line TDC

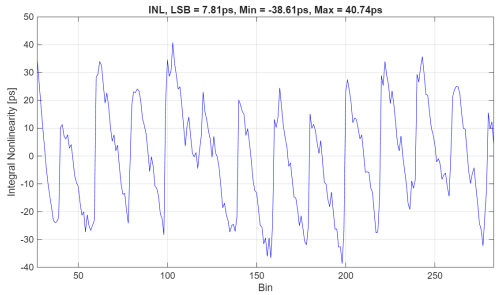

Figure 2: Linearity of a ressource-optimized TDC

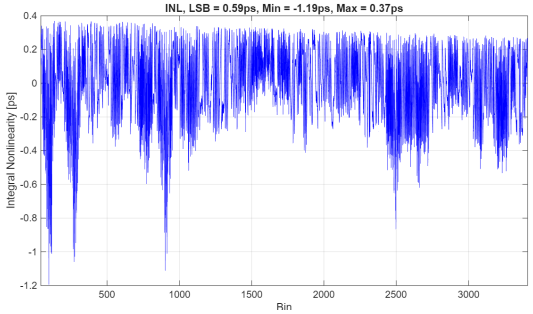

Figure 3: Linearity of a performance-optimized TDC

Working Principle

A simple and widely used architecture for implementing TDCs in FPGAs is the Tapped-Delay-Line (TDL) TDC. The signal to be measured is passed through a chain of identical delay elements (delays). After each delay element, the chain is connected to the input of a FlipFlop. At regular intervals, triggered by a clock signal, the FlipFlops record the current state of the chain. The resulting state is then evaluated by an encoder and the digital time value is calculated.

Implementations

TDCs have already been successfully implemented on a variety of different FPGAs at IMES. FPGAs from the Xilinx family (7-Series, UltraScale+), Intel (Cyclone V, Arria 10) and Efinix (Titanium) have been used. The requirements ranged from a fine time resolution below 2 ps and an accuracy better than 10 ps to pulse detection with possible frequencies above 1.5 GHz. Different TDC architectures were realized. These ranged from classic carry-chain-based TDCs to novel delay chains based on DSPs.

In-Depth Knowledge

Thanks to the in-depth knowledge at IMES of the structure and physical behavior of FPGAs, the TDCs could be optimized for each specific architecture in terms of their positioning within the FPGA and with regard to nonlinearities. Various correction algorithms also enable internal real-time calibration of the TDCs directly in the FPGA and allow for temperature-stable operation.

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