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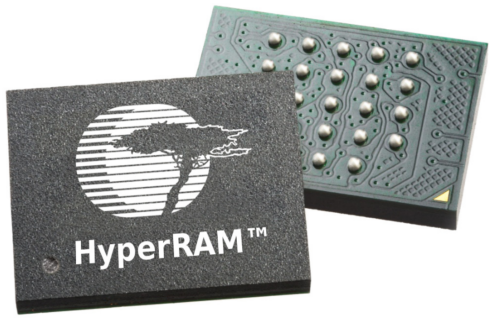
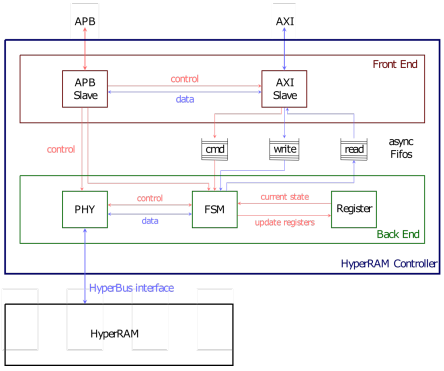
Topic	Sensor, Actuator and Communication Systems
Project Partners	u-blox Holding AG , Thalwil , ZH

HyperRAM Controller

Design and implementation of a HyperRAM controller



HyperRAM chip



HyperRAM controller block diagram

Introduction: Mobile devices become smaller, and have more computational power from generation to generation. To achieve the required performance, a continuous improvement and optimization is needed. Not only CPUs have to become better, but also eht entire system performance has to improve in order to be able to develop devices for the future. Memories are used in each of these to store data. This thesis deals with high performance, low power memories. For this type of application, a Pseudo static RAM (PSRAM) is often used. This is a dynamic RAM with an internal refresh logic. Seen from the outside, the device can be used as if it was a static RAM.

Objective: The company u-blox uses CellularRAM for one of their chips at the moment. CellularRAM is a type of PSRAM. To be flexible and ready for the next generation of low power memory devices, HyperRAMs shall be investigated. HyperRAMs is a PSRAM device as well, but works with an interface called HyperBus. In a literature review, a comparison between HyperRAM and CellularRAM shall be done. The following characteristics have to be studied:

- Signal count
- Power consumption of the memory
- Data exchange speed between a memory and a controller

Only a high performance controller can deal with high performance data buses. Therefore, memory controllers shall be studied in a second step. Such a controller has to be developed for a HyperRAM. u-blox has already implemented one for the CellularRAM. The Front end of this controller interfaces an AXI and an APB bus. AXI is used for high data throughput and APB for configuration of the memory controller.

Result: The CellularRAM interface and the HyperBus were compared. These bus systems vary not very much in terms of data rate. Power consumption turned out to be lower for the CellularRAM. The big advantage of HyperBus, however, is the low signal count. Whereas a HyperRAM interface needs at maximum 13 Pins, a cellularRAM with the same memory size needs at least 31. A HyperRAM controller was developed in this thesis. It was separated into a Front and Back end part. A first version of the Back end could be implemented successfully. Front and Back end work in two different clock domains. Clock domain crossing was an important issue, which was solved with an asynchronous FIFO. For the generation of the required double data rate (DDR) signal, an existing DDR cell was used. For synchronization, a delay locked loop (DLL) was used.