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Subject Area	Sensor, Actuator and Communication Systems
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Advanced Hallsensor

Concept, System & Analog Frontend Design

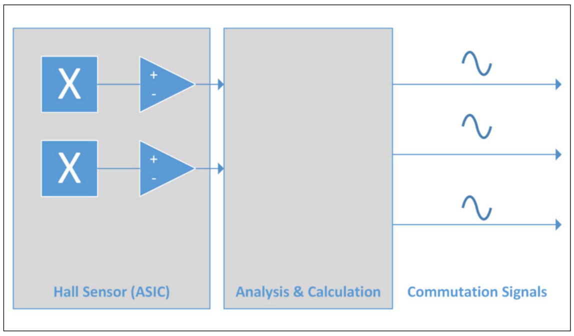

Figure 1: Concept

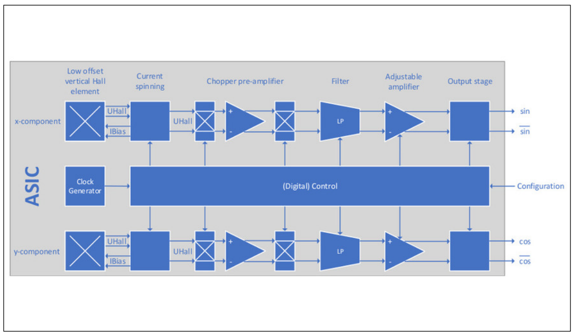

Figure 2: System Design

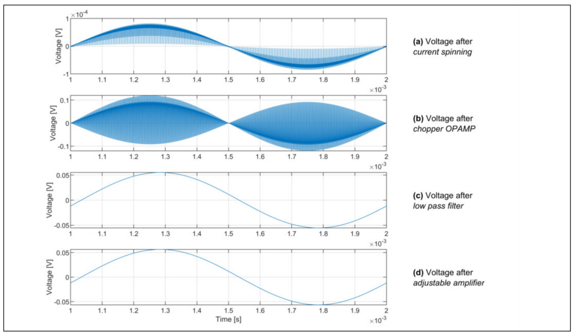

Figure 3: Simulation of Analog Design

Introduction: The German company Dr. Fritz Faulhaber GmbH & Co. KG is specialized in miniature and micro motors. Faulhaber motors are available with a variety of sensors and encoders for providing solutions to a wide range of drive applications. These motors contain an integrated analog or digital Hall sensor which senses the magnetic field of the rotor in order to generate the output commutation signals. Hall sensors precisely switch the pole changes relevant for the respective commutation steps. As the number of rotor poles increases, the demands on the quality of the commutation signals increase drastically, as do the tolerances of the individual parts and their mounting brackets.

Objective: The objective of this work is to develop a novel ASIC. This ASIC should contain two vertical Hall elements and generate three identical sinusoidal signals, which are 120°e phase shifted from each other. Moreover, the phase shift and amplitude of these signals should also be freely configurable in order to reduce the tolerance requirements and therefore bring more flexibility in comparison to the existing sensor system.

Procedure / Result: In a first phase, the basics of Hall elements and encoder technology were acquired. Subsequently, various implementation concepts were evaluated in an analysis and a system design was created. All required hardware blocks were evaluated for advantages and disadvantages as well as for possible problems. Simulations of the behavior of the magnetic field of an encoder rounded off this analysis phase. This acquired knowledge made it possible to develop a theoretical design using VHDL AMS. From this design, further important insights into the functionality of the system could be gained and the system design was improved accordingly. In the next phase the CMOS design was created. At the same time, the functionality of all implemented blocks was tested by means of simulations.

In the scope of this work the analog frontend was developed for the ASIC. This includes the possibility to amplify the measured Hall signal and to eliminate any offset voltage. The final amplification of the signal is configurable. The entire analog design is also designed for a temperature range of -40°C to 150°C and a voltage range of 2.5V to 5V.