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Subject Area	Sensor, Actuator and Communication Systems

600 MSample/s ADC in an FPGA

A fully flexible, novel ADC without any external components

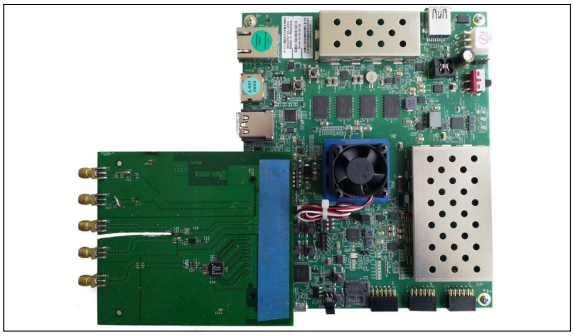

Figure 1: FPGA board connected to the test board.
Own presentment

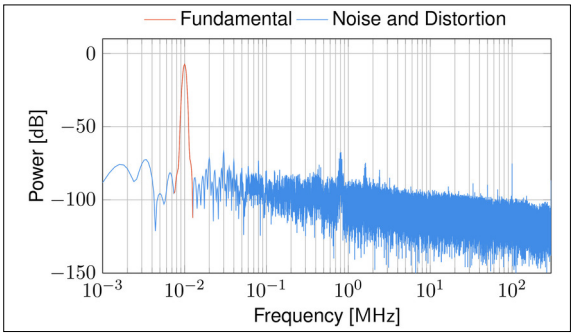

Figure 2: FFT spectrum of 10 kHz sine as measured by the ADC. The SINAD is 43.3 dB.
Own presentment

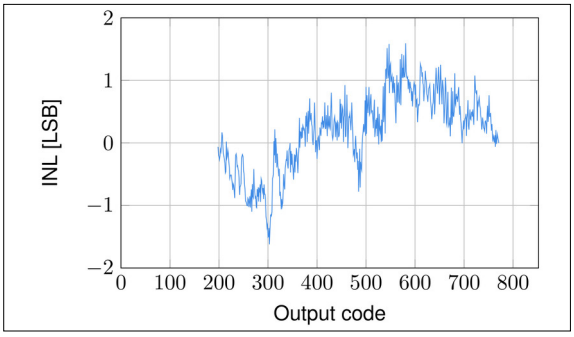

Figure 3: Integral nonlinearity of the ADC.
Own presentment

Objective: In today's world, analog-to-digital converters (ADCs) are essential. Numerous applications need such a conversion, for example analog sensors whose signals are further processed digitally. Current trends show that analog signals are digitized earlier and earlier in the processing chain to benefit from less analog signal processing. ADCs exist in numerous implementations to cover a wide range of specifications. They exist as standalone components or are integrated into field-programmable gate arrays (FPGA) or microprocessors.

However, such ADCs are designed for a specific set of requirements with limited flexibility. Latest publications show the possibility to implement an ADC directly in an FPGA using the reconfigurable logic blocks. These ADCs are based on the slope ADC and measure the time from the start of a reference slope until that slope reaches the voltage to be measured. The time can be measured with a time-to-digital converter (TDC). Advantages of such ADCs are that they require hardly any additional external elements and that they can be adapted to a wide range of requirements.

The objective of this work is to develop a novel ADC that no longer requires external components. Furthermore, additional error correction schemes shall be evaluated and implemented to offer a wide range of settings. This would allow to use the ADC in a broad range of applications.

Approach: In a first phase, a reference ADC that requires external components was built. In parallel, a simulation model of the ADC was created to gain further insights. The structure of the reference ADC was then changed to remove the need for external components. Two different implementations were developed in order to cover different types of FPGAs. In a third phase, correction schemes were evaluated and implemented to increase the linearity and resolution of the ADC. Finally, all ADC versions were tested and specified in a fully automated measurement setup.

Result: A novel structure of FPGA based ADCs was developed. The ADC is fully reconfigurable, does not require any external components, and is built using only FPGA internal elements. Two different reference slopes were implemented to support different FPGAs. One reference slope is generated with a simple step. A pattern generator helps to create the second reference slope by using the parasitic capacitance of the FPGA pad which integrates the generated pattern. The generator itself is able to create an arbitrary pattern in the FPGA with a speed of up to 10.8 Gbit/s.

The 8.8 bit ADC achieves an effective number of bits (ENOB) of 6.9 at a sampling rate of 600 MSample/s and an ENOB of 5.1 at 1.2 GSample/s. The input voltage range reaches from 0.15 V to 1.45 V. There are no missing codes in the ADC. The differential nonlinearity (DNL) ranges from -0.8 to 1 bit, and the integral nonlinearity (INL) is in the range between -1.6 and 1.6 bit.