Parasitics in Parallel Hard Switching Silicium-Carbide MOSFET Applications

Graduate

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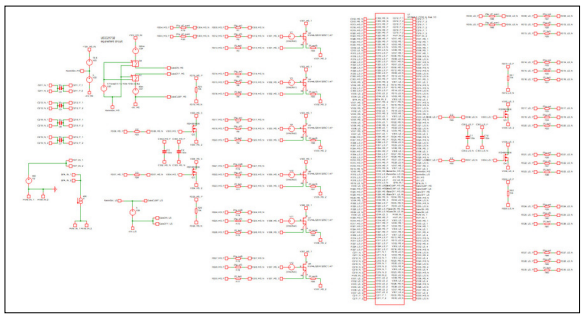
Introduction: To increase the driving range of an electric vehicle, hard switching motor inverters are used. Hard switching inverters are the standard in the automotive industry and highly efficient. To reduce losses in the inverter, the switching speeds are very high. This advantage is difficult to achieve because high switching speeds lead to undesirable parasitic effects. These are caused by the, in this case, high rates of change of the currents and voltages involved. They interact with the parasitic elements of the PCB and the components and cause parasitic turn-ons or ringing. To prevent these effects, a deep understanding of these parasitic elements is required in order to mitigate them in the first place. These problems are compounded when in order to increase the power rating of the inverter, the switching devices are connected in parallel to increase the current capability.

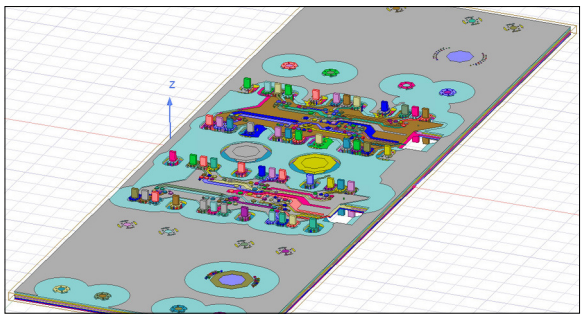
Approach: In this thesis the layout of a given inverter is taken and the parasitics are extracted in FEM simulations. The investigated inverter layout is provided by BRUSA Elektronik AG. The performance targets to reach are 850V DC-link voltage and a continuous phase current of 400A RMS. This at a switching speed of more than 20V per nanosecond. The extracted parasitics are used to build a simulation model. This model is used to perform transient simulations of the switching behaviour of the inverter. With the knowledge gained from the extraction of the parasitics and the transient simulation a new and improved layout is created. The parasitics of this layout are then also extracted and transient simulations are performed. The results of these simulations are then compared with the old results and used to further improve the layout.

Result: The process from a layout to the extracted parasitics is challenging and difficult to optimize. Many steps are required to make the workflow not only usable, but also simple and fast. The process is finally optimized and results can be obtained in a short time. Another challenge is the use of the extracted parasitics in transient simulations. The parasitics are exported as SPICE netlists and used in a SPICE solver. This process is surprisingly simple and working on the first try. Due to the long simulation time of this complex and large equivalent circuit, the original model is simplified, resulting in smaller SPICE netlists. The procedures described above are finally used to improve the given layout and to create transient simulations from it as well. The changes and improvements in switching behaviour of the reworked model are clearly visible. The results are very promising and the switching behaviour of the new layout is very good. Based on this layout, a prototype is later produced to verify the simulated performance. If the performance of the prototype is acceptable a full product is developed on this basis.

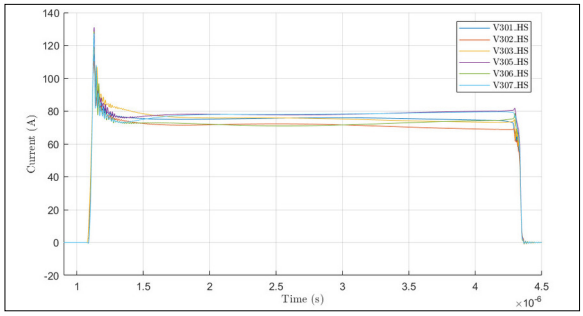
Transient Simulation Circuit
Own presentment



Simulation Model
Own presentment



Semiconductor Currents
Own presentment



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Subject Area
Energy and Environment