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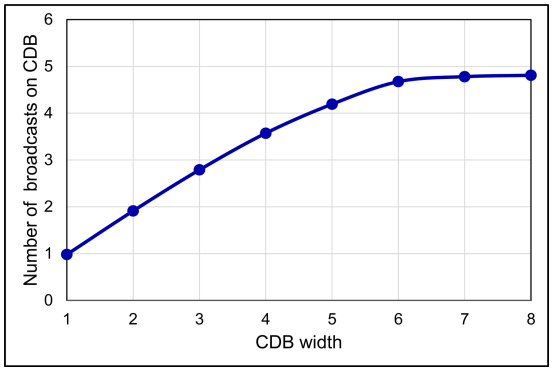
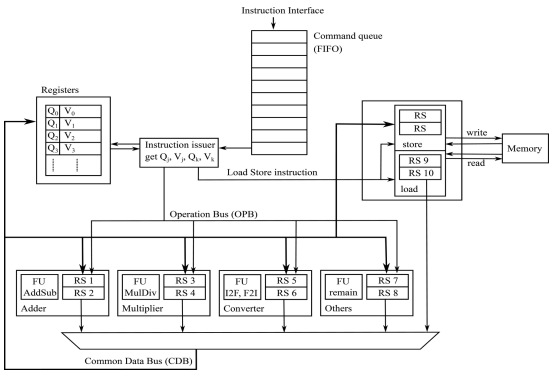
Vector Floating Point Unit

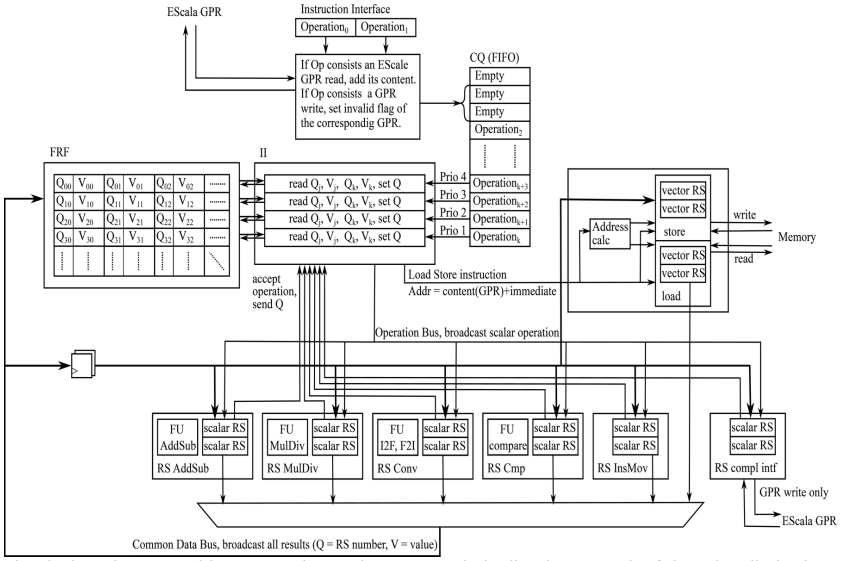
Architecture of floating point unit supporting vector instructions and hardware parallelization by using Tomasulo's algorithm



Performance result of a random test program. The VFPU size is increased by parameters. Its throughput rises up to a certain point.



Tomasulo's algorithm was introduced in1961. It is still one of the best architectures for dynamic scheduling.



The designed VFPU architecture. It instantiates several pipelined FPU. Each of them has limited functionality.

Ausgangslage: The product portfolio of Esencia Technologies includes a fully configurable very long instruction word processor, named EScala. Depending on customer requirements, the EScala system includes different IP blocks for DSP and security applications. Each of these IP cores can be configured individually. An important block of the processor is the floating point unit (FPU). Until now, an iterative block has been used. Depending on the application, the FPU has been a bottleneck in the EScala system even if it was instantiated several times.

Vorgehen: A high performance subsystem replacing the iterative FPU shall be designed. The subsystem shall instantiate several pipelined FPUs. Each of the FPUs shall support just a few operations. The subsystem shall interconnect and organize different floating point blocks in such a way that individual units can be highly utilized. The subsystem shall support both vector based and scalar based operations. It shall contain its own registers as well as interfaces for external memory. To fit in the EScala system, the design shall be configurable for different requirements.

Ergebnis: A vector floating point unit (VFPU) processor has been designed. Although its instruction set is vector based, only parts of the design are vectorized internally. The main part is based on Tomasulo' scalar architecture. This allows for execution of instructions out of program order. The so called dynamic scheduling increases throughput by raising the utilization of the specialized, pipelined FPU blocks. The VFPU is highly parameterized. The VFPU can be adapted to user needs within short time: different parameter settings offer great variability from a compact IP block fitting in a small FPGA to a high performance block, which processes several instructions every single clock cycle.