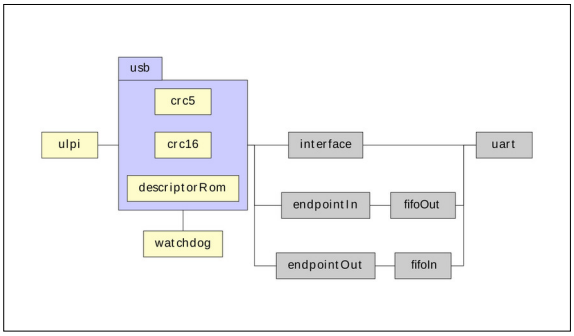
Pascal Stump

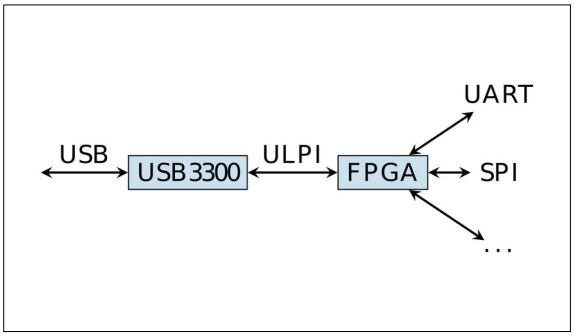
Student	Pascal Stump
Examiner	Prof. Dr. Paul Zbinden
Subject Area	Innovation in Products, Processes and Materials - Industrial Technologies
Project Partner	Enclustra GmbH, Zurich, ZH

USB 2.0 ULPI Device

A VHDL Design for USB 2.0 with a ULPI Connected PHY



VHDL block overview



Communication overview

Introduction: Enclustra GmbH is a dynamic, innovative and successful FPGA design service company located in Zurich, which provide services covering the whole range of FPGA-based system development. In the FPGA Solution Center, Enclustra develops and markets highly-integrated FPGA modules and FPGA-optimized IP cores. The Enclustra FPGA modules and baseboards often contain a USB device, which is used to configure the hardware and for communication between the FPGA/SoC and the host PC. At the moment a FTDI FT2232H USB chip is used for this communication. Because the FT2232H only supports two protocols simultaneously, a lot of multiplexers are needed to support all required protocols. The task of this project is to implement a USB device to use the full capacity of the USB connection with the potential of having multiple protocols at the same time. The USB3300 should be used as a PHY chip which has a ULPI interface.

Procedure / Result: At the beginning of this project, a set of basic requirements were discussed with the industrial partner, to learn the needs and wishes. With these basic requirements—COM ↔ UART communication, wrapper library for other protocols and 32 bit/64 bit support—the USB specification was used to create a design, which was then implemented and verified on the real hardware.

Result: The relevant parts of the USB specification were aggregated into a chapter of the project documentation, in order to get into the subject more easily. The benefit of the newly created VHDL design of a composite USB device, is the flexibility to add/change various protocols. To take advantage of the full ability of USB 2.0, some small extensions are required in the actual full-speed design. The implementation reached the status, that a host should detect the right kind of the device and its construction. Unfortunately the test on the real hardware did not work. It seems that the clock driver of the used USB3300 is unable to drive the long wire from baseboard to FPGA input. A possibility to avoid this problem would be to create an adapter board with the USB3320, which could work with a clock driven by the FPGA. The use of libusb is suggested for the communication to non-standard USB class protocols. This makes it unnecessary to implement own operating system drivers.