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IP Protection by Watermarking
Combinational Logic Synthesis Solutions

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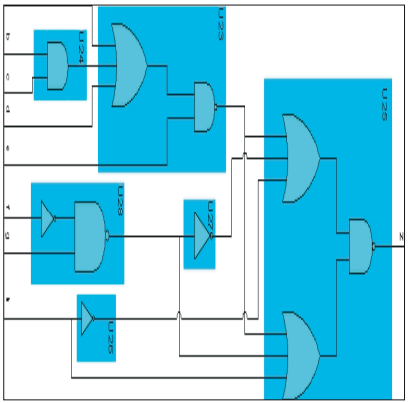
Subject area	Embedded Systems, IP–Watermarking
Project partner	NTU, Nanyang Technological University NTU, Singapore

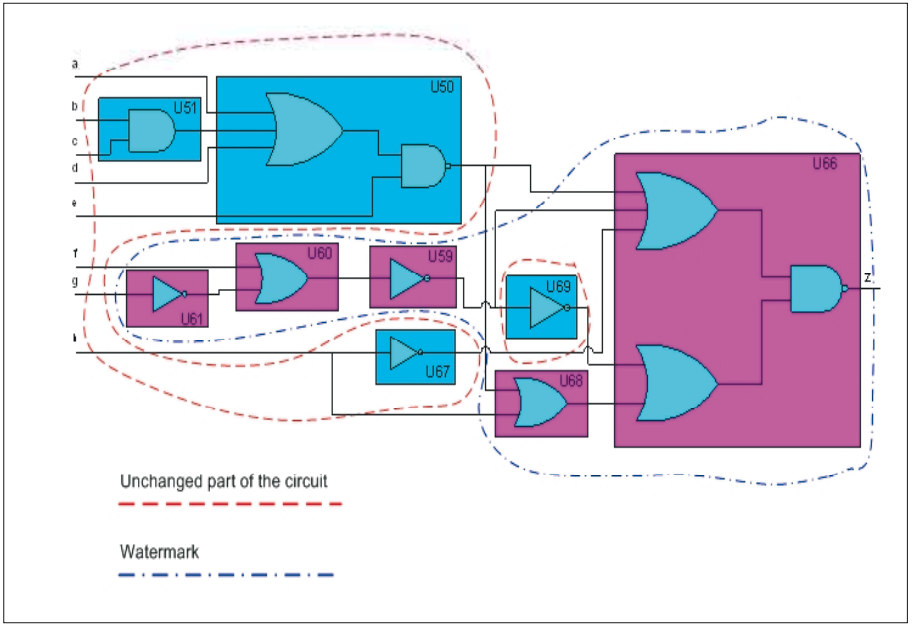


Unmarked circuit

Problem: In this project, the focus is an approach to IP protection which facilitates design watermarking at the combinational logic synthesis level. We will study a method to achieve strong proof of authentic ownership without adversely influencing VLSI performance metrics, such as timing, area and power. The main tasks include: implementing the watermarking scheme at the combinational logic synthesis level, testing the watermarking method on a standard set of real-life benchmarks, and demonstrating the strength of watermarking when applied to proof of authorship.

Project Targets:

- Improve the knowledge of watermarking algorithms
- Become familiar with synthesis tools (Synopsys Design Compiler)
- Find a way to extract some watermarks out of a marked circuit



Circuit with a watermark

Current Situation: At this point of time, there is no useful method available to set and extract watermarking in IP (intellectual property). If we (the NTU Team and I) succeed, the results of our project could have a major impact on the whole chip industry.

Proposed Solution: A possible way to solve the problem of watermark extraction is to find a unique value for each of the chosen kernels. This value should be the same both before and after the watermarking process. This appears to be the easiest way to identify a watermark in a marked circuit.

It is not yet possible to forecast whether the proposed solution will solve the given tasks, because we are still the process of finding such unique values. But we are very optimistic that this attempt will solve some of the problems around watermarking combinational logic IP.