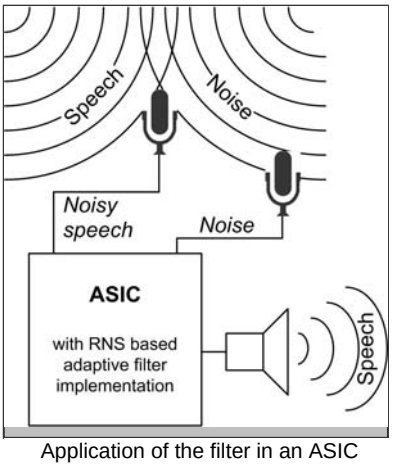
Design of a RNS based adaptive filter

In cooperation with Nanyang Technological University, Singapore

Yves Huber *Patrick Morger*

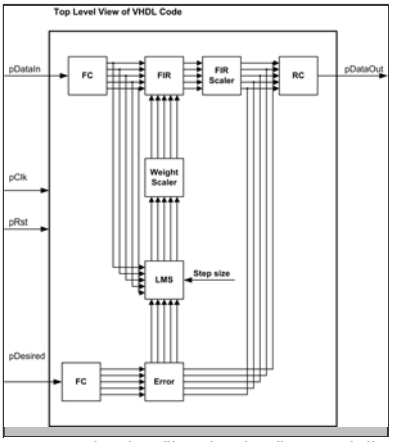
Diplomanden	Yves Huber; Patrick Morger
Examinator	Prof. Erwin Brändle Assoc. Prof. Dr. Chip-Hong Chang NTU
Experte	Theo Scheidegger
Themengebiet	High Performance Embedded Systems
Projektpartner	Nanyang Technological University, Singapore



Application of the filter in an ASIC

Problem: Adaptive filters are highly used in modern communication systems such as mobile phones or digital radio receivers. They work as noise suppressors on the simple, but powerful Least Mean Square (LMS) algorithm. For further increasing of transfer rates new implementations of these filters are needed. The challenge is the combination of high throughput rates along with small silicon area usage and low power consumption. Today's developments are using the Residue Number Systems (RNS) to combine the different attributes and requirements. RNS is known for its inherent characteristics of carry-free operations, high parallelism capability and great fault tolerance.

Project Goal: The aim of the thesis is to implement the first, completely RNS based, adaptive filter system. The first step is to program the filter in VHDL code. In a second step, the entire implementation has to be tested with ModelSim to proof its operational reliability. Future projects after the thesis could focus on implementations on an Application Specific Integrated Circuit (ASIC).



RNS adaptive filter for the five moduli

Solution: New inventions are worth nothing without an accurate implementation. Therefore the specifications of the filter and its application had to be defined first. Then an adaptive filter in binary system was built, to be able to compare with the RNS filters later. It was important to get familiar with the influence of truncation and scaling, due to the iterative behaviour of adaptive filter algorithms.

A top to bottom design in VHDL was designed, followed by the implementation of the different VHDL-modules like Forward Converter (FC), Residue Arithmetic Unit (RAU) and the Reverse Converter (RC). The Forward Converter converts the binary input to the corresponding residue presentation. The FC is based on the new moduli set $\{2^n-1;2^n;2^n+1;2^{n+1}-1;2^{n-1}-1\}$ proposed by the Nanyang Technological University (NTU). In the RAU all calculations for the Finite Impulse Response (FIR) filter as well as for the LMS algorithm are done. Finally the Reverse Converter converts the residue value of the filter output into the corresponding binary representation.

This diploma thesis was written at the Centre for High Performance Embedded Systems (CHiPES), an institute of the Nanyang Technological University under a well established student exchange program. This mutual program offers the students great opportunities to increase international experience and relationships, as well as getting in touch with different cultures.