Performance analysis of FIR filter synthesis and optimization algorithms

In cooperation with Nanyang Technological University, Singapore

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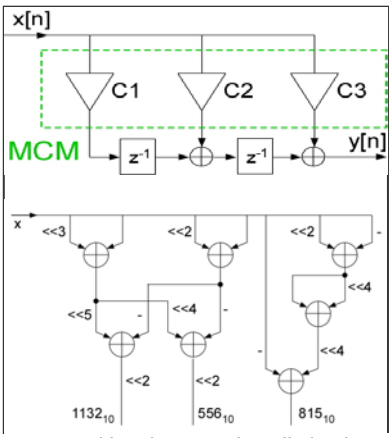
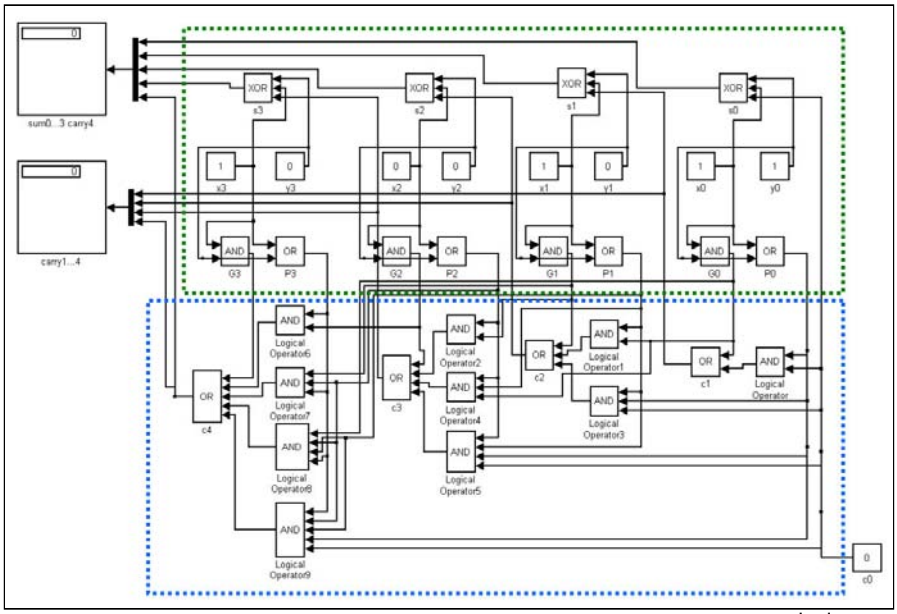
Problem: Finite Impulse Response (FIR) Filter are used in almost every application containing digital signal processing. Being able to analyze the performance is essential for comparison and optimization.



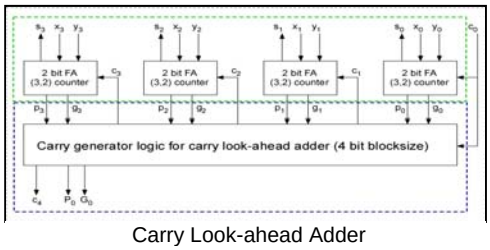
MCM with subexpression elimination

Project Goal: Multiple Constant Multiplier (MCM) blocks are the most cost intensive part of a FIR filter in terms of silicon area needed and delay. MCM blocks can be implemented using different adder types. To compare these implementations, the total number of discrete adders has been used up to now. In this project the number of Full Adders (FA) and logic gates is used as granular unit.

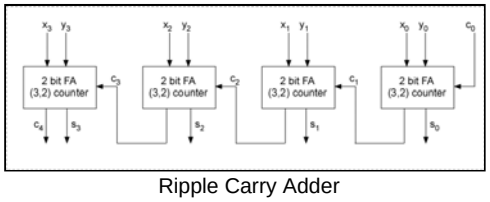
Solution: For this project a FA, Half Adder (HA) and logic gate count for Ripple Carry Adder (RCA) and Carry Look-ahead Adder (CLA) have been evaluated and used in a Matlab® file to calculate area and delay costs. Using these results allows implementing FIR filters in a hybrid adder structure, achieving an optimization in area or delay. Using a standardized format (sysFIR) enables a generic calculation for any FIR filter supporting this format.



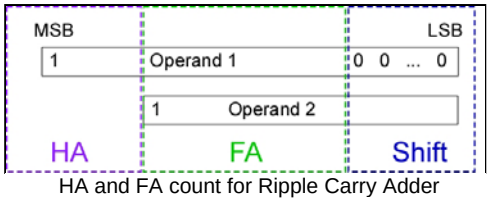
4 bit blocksize Carry Look-ahead Adder in logic gate count, including the carry generator logic



Carry Look-ahead Adder



Ripple Carry Adder



HA and FA count for Ripple Carry Adder