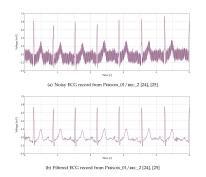


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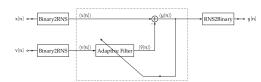
Subject Area

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Design of Low-Power Modulated Filter Banks for Electrocardiogram Feature Extraction



Comparison of a noisy (a) and filtered (b) ECG signal.



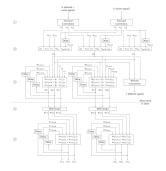
Introduction: In recording Electrocardiogram (ECG) signals, a crucial problem is the appearance of artifacts (noise). The most common artifact in ECG signals is the so-called power-line interference. Therefore, this research looks into an efficient filter design to suppress the power-line interference of ECG signals. The approach to this problem is new and crucial in reducing the hardware cost and power consumption of the Digital Signal Processing (DSP) operations in ECG signal processors.

Many different filter designs have been proposed over the last decades, covering a broad range of performance characteristics. In the context of this research, an adaptive digital filter based on the Residue Number System (RNS) representation for suppressing the power-line interference in ECG signals is simulated and designed. Besides, the proposed design is not in a hybrid form. Thus, all of the computations are done in the RNS representation.

Proceeding: First, various simulates of different digital filters in the conventional and RNS representation were performed in Matrix Laboratory (MATLAB). Afterwards, the most appropriate method with the best results was picked. Second, an efficient digital circuit, described in Hardware Description Language (HDL), was developed upon finalizing the design based on our proposed algorithm. The last step was to perform the technology mapping of the design to standard Complementary Metal Oxide Semiconductors (CMOS) cell libraries. This step enabled the estimated silicon area cost, chip power consumption, and delay of the design.

Result: With this research, a non-hybrid functional RNS-based adaptive filter was developed to suppress the power-line interference in ECG signals. Also, a new architecture has been proposed which does completely all of the operations in the RNS representation. It is shown that the estimated silicon area cost, chip power consumption, and delay of this architecture can keep up with the best solutions in the literature.

RNS-based adaptive noise canceler, where x[n] is the ECG signal, v[n] is the noise signal, and y[n] is the noise-free output.



HDL architecture of the proposed RNS-based adaptive noise canceler.