Design of a fully integrated Buck-Boost Converter ASIC

A small Buck-Boost Converter ASIC with integrated switches on a commercial 0.35 um process node

Students

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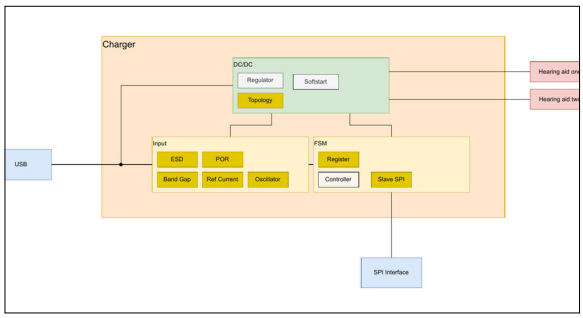
Introduction: This part of the project focuses on the pre-layout phase of a project, which was divided into pre-layout and post-layout stages. The project was initiated by Sonova AG, with the objective of designing a compact 200 mA DC/DC converter for the potential integration into the charging case of their hearing devices. The device should generate a stable 5 V supply from a USB power source with a input range of 4.35 V to 5.5 V, in accordance with the USB specification. In addition to the analog circuits in the switching converter, a digital SPI interface was added which allows for digital modification of the device settings.

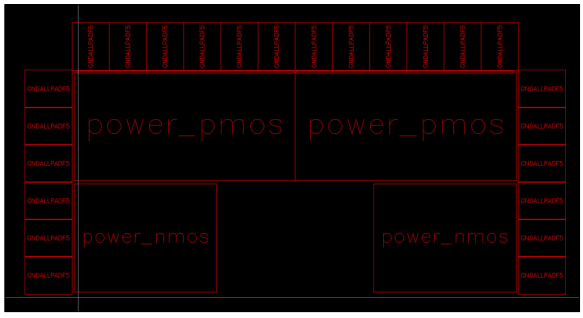
Approach: We decided to build the ASIC on the mature 0.35 um process from X-Fab. The 0.35 um process was selected due to its availability as a multi-project-wafer (MPW) and its suitability for analog circuit design. The switching converter uses the peak current mode control technique. The inner control loop regulates the peak current flowing in the inductor, while the outer control loop gives it its set point. The outer loop regulates the set point of the inner loop based on the voltage measured at the output of the device. If the voltage at the output is too low, it increases the current flow in the inductor, thus raising the output voltage. Various safety features such as thermal shutdown, soft-starting and a short circuit resistance were implemented. A large portion of the chip area is devoted to the four large power transistors, which need to be able withstand currents of over 400 mA, when under maximum load. All analog circuits such as OTAs, oscillators and voltage references were designed or adapted by ourselves, as the circuits available in the our component library are not suitable.

Conclusion: The ASIC we designed was able to meet our specifications in simulations and achieved an efficiency of greater than 90% under full load. Due to time constraints we were not able to complete the layout of the chip during this thesis and had to postpone the tape out. We will be continuing to work on this ASIC as part of our next thesis, where we finish the design, test and characterize the finished ICs.

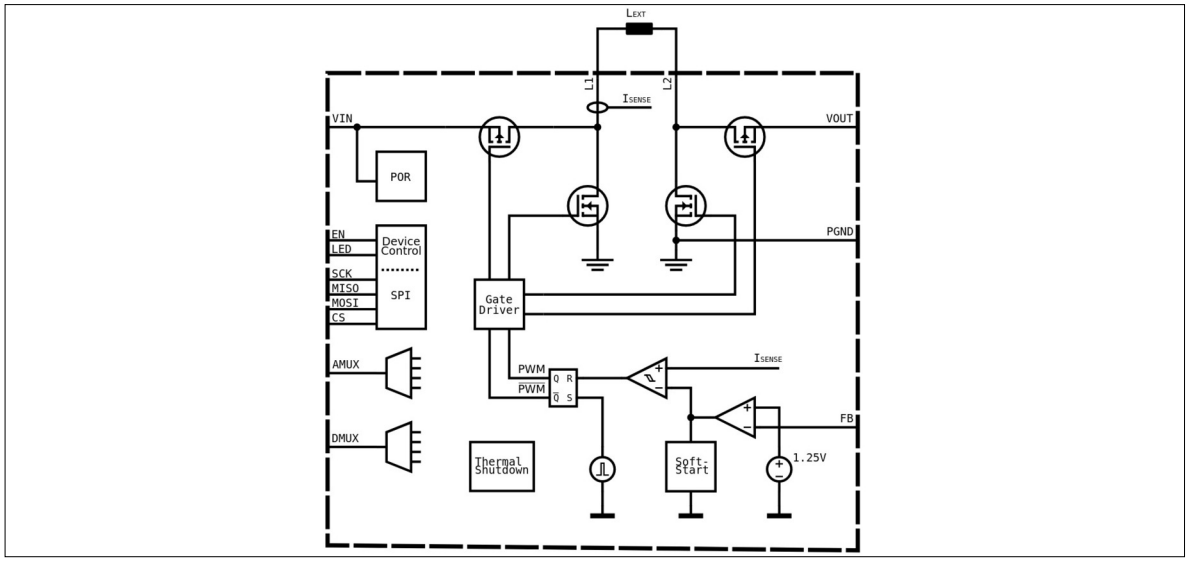
Architecture overview of the chip
Own presentment



Layout of the high power transistors
Own presentment



Functional Block Diagram of the Chip
Own presentment



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Subject Area
Electrical Engineering