Semantic VHDL Code Formatter

Students

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Introduction: VHDL is an established hardware description language used in safety- and reliability-critical digital design. Despite its continued relevance, modern tooling support is weak compared to other languages, especially regarding automatic formatting and integration into automated workflows. There is currently no widely adopted formatter that enforces consistent coding conventions for VHDL projects.

Approach / Technology: This project presents a standalone command-line VHDL formatter based on a structured parsing and pretty-printing pipeline. ANTLR is used to generate a concrete syntax tree from an existing public VHDL grammar, which is then mapped to an abstract syntax tree tailored for deterministic formatting rather than full semantic analysis. Code generation relies on a document-based pretty-printing approach inspired by Wadler's layout algebra, enabling consistent indentation, line breaking, and alignment. The formatter is configurable, allowing adaptation to project-specific style rules instead of enforcing a single convention.

Conclusion: The formatter already supports a substantial subset of VHDL and produces clean, consistent output regardless of input quality. Although full VHDL-2008 coverage is still under development, future work focuses on extending language support, providing cross-platform binaries, and integrating the tool into editors to support streamlined and maintainable VHDL development.

Before formatting
Own presentment

```
entity benchmark_entity is
    generic (
        WIDTH : integer := 32
    );
    port (
        i_clk : in  bit;
        i_rst : in  bit;
        i_en : in  bit;
        i_data_in : in  bit;
        o_data_out : out bit
    );
end benchmark_entity;
```

After formatting
Own presentment

```
entity benchmark_entity is
    generic ( WIDTH : integer := 32 );
    port (
        i_clk      : in  bit;
        i_rst      : in  bit;
        i_en       : in  bit;
        i_data_in  : in  bit;
        o_data_out : out bit
    );
end benchmark_entity;
```


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Subject Area
Software, Software Engineering