Synchronous Rectifier

Synchronous Rectifier for cochlea implant

Graduate

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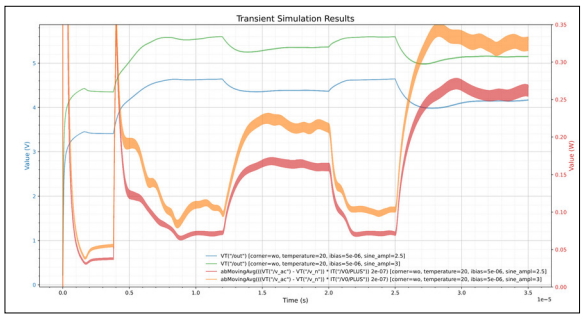
Introduction: Wireless power transfer for medical implants requires high-efficiency rectifiers. Conventional passive rectifiers are limited by diode forward voltage drops, which cap their efficiency. Synchronous rectifiers use low-resistance MOSFETs to reduce this conduction loss. This approach introduces power overhead from two sources: the quiescent consumption of the control system and the dynamic switching losses required to drive the MOSFET gates. At the operating frequency of the target cochlea implant, these switching losses become a dominant factor, creating a critical trade-off that defines the rectifier's viability.

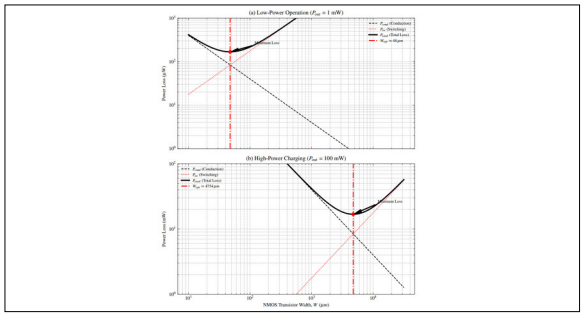
Objective: The primary objective is the design and feasibility evaluation of a two-transistor Delon synchronous rectifier in a 0.18 µm CMOS process. This requires developing a feedback-based adaptive control architecture, as shown in the system diagram, to manage sub-nanosecond switching delays. A key task is to perform a quantitative analysis to model the relationship between transistor width, conduction loss, and switching loss, as illustrated in the power loss plots. This model will identify the optimal operating point for different loads. The final goal is a comparative evaluation to determine if the integrated design achieves higher overall efficiency than a discrete Schottky diode solution.

Result: The control architecture was successfully designed and verified. Transient simulations confirm robust startup sequences and stable operation under dynamic 20 mA and 40 mA load steps across all process, voltage, and temperature corners. The power loss model was validated; for the target 1 mW application, the optimal transistor width is small (~48 µm), where the system's high quiescent power and switching losses dominate. For a 100 mW high-power scenario, the optimal width is much larger (~4754 µm). The synchronous rectifier's maximum theoretical efficiency of 70.4% was found to be lower than a discrete Schottky diode's (86.2%). The architecture is therefore not viable for the target application but it could be suited for other high-power scenarios, with some modifications, where control overhead is less significant.

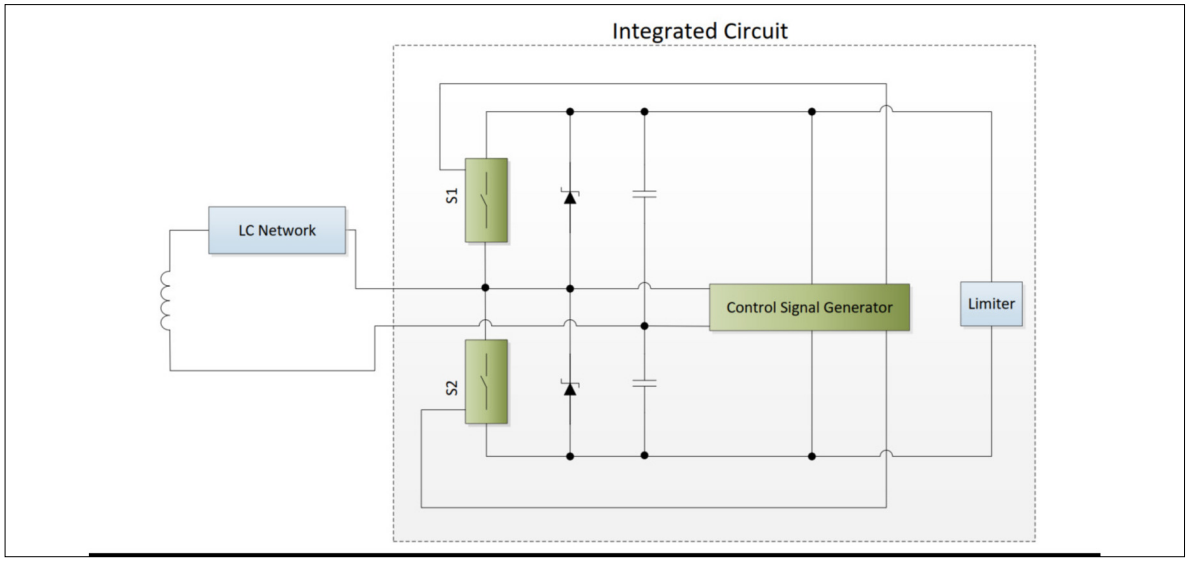
Top-level transient simulation showing the controlled startup sequence.
Own presentment



Plot of conduction, switching, and total power loss as a function of NMOS transistor width.
Own presentment



The simplified proposed architecture, illustrating the PMOS and NMOS switches.
Own presentment



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