Time to Digital Converter

A multi-channel implementation on an FPGA

Students

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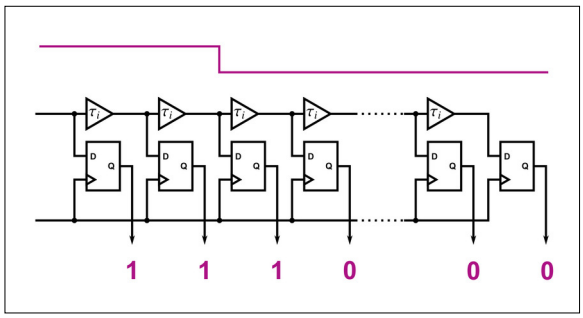
Introduction: Fluorescence Lifetime Imaging Microscopy (FLIM) can be used as an imaging technique to visualize cell activity. For that purpose, a laser diode fires a beam at a fluorescent sample material (fluorophore), which absorbs the energy by leveraging one of its electrons into a higher energy state. After some time, the electron falls back into its previous energy state and emits a photon by doing so. This emitted photon is then being captured by a photon detector. For each detected photon, the detector emits an electrical pulse. Those pulses are then transmitted to the PCB developed in this thesis. From a research point of view, the timing of those pulses is of interest to determine the lifetime of the fluorophore to eventually get insights of the cell's activity. As the required time stamp accuracy is in the range of 100 ps, a classical counter is not feasible. Hence, a Time-to-Digital Converter (TDC) is used.

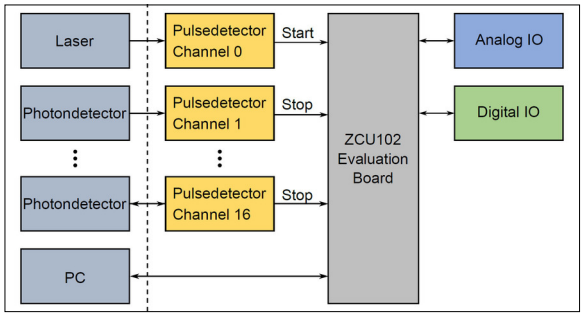
Approach: One common way to implement a TDC is to use a Tapped Delay Line (TDL) as has the IMES already done multiple times. For this, the carry chain of an FPGA is used as a delay line to provide sub-clock resolution. In this thesis, such a TDL has been used to develop a multi-channel TDC on an FPGA. Thanks to the multi-channel approach, it is possible to use multiple detectors at the same time, thus improving the performance of the measurements. As there were already multiple previous projects available at the institute, the first step was to gain an overview over the current state. Next, the required components for a multi-channel design were identified and specified. During the following design phase, the specified parts were integrated into a PCB design. The challenge was to fit all 17 pulse detection circuits and the additional user inputs and outputs onto a PCB while maintaining signal integrity.

Conclusion: This thesis showed that it is possible to create a 17-channel high precision TDC on an FPGA. The best achieved standard deviation for a single channel was 15 ps without any additional calibration. To further increase the performance of the system, multiple improvements have been identified.

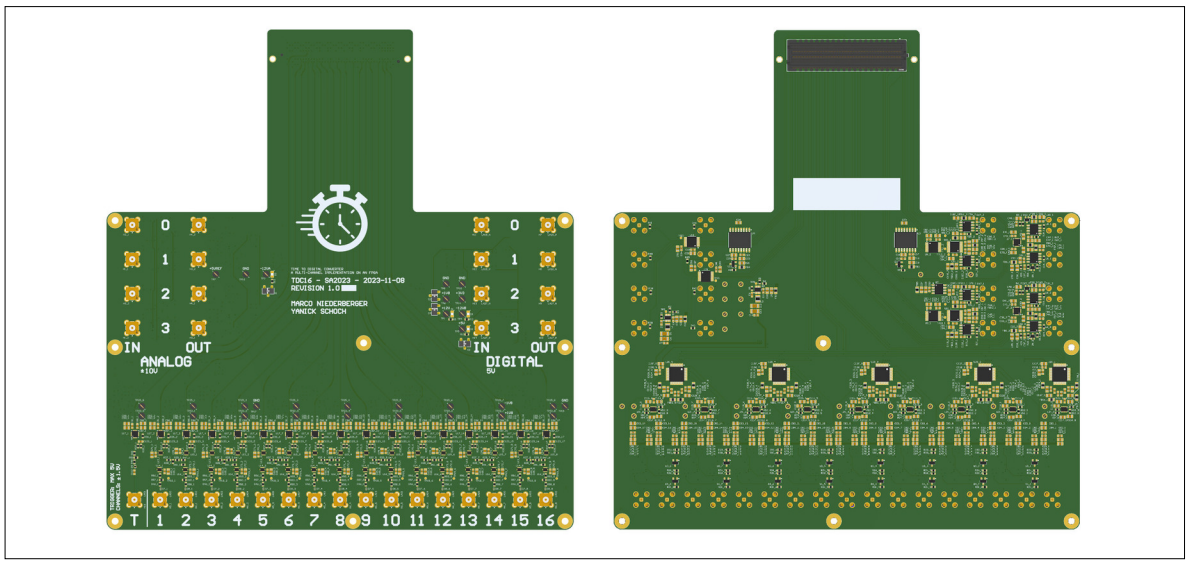
Tapped delay line using delay elements and D-Flip-Flops to sample the propagated signal through the carry chain.
Based on S. Henzler, Time-to-digital converters: Springer



All implemented subsystems with the measurement channels on the left side and the user IO on the right side.
Own presentment



The developed PCB with the 16 measurement channels on the bottom edge.
Own presentment



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