A High-Bandwidth, Sub-Femtofarad Capacitive Sensor Frontend

Implemented in 0.35um CMOS Technology

Student

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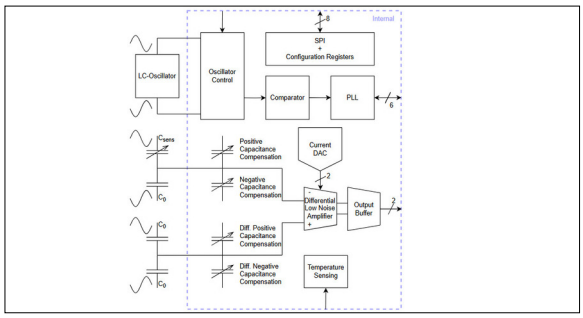
Introduction: Accurate measurement of extremely small capacitance differences is essential in a wide range of high-performance sensing applications, including gyroscopes, accelerometers and fingerprint sensors. The goal of this master project thesis is the design of an application specific integrated circuit (ASIC) for measuring capacitance differences from 1 aF up to 25 fF with an excitation signal frequency of 12.5 MHz.

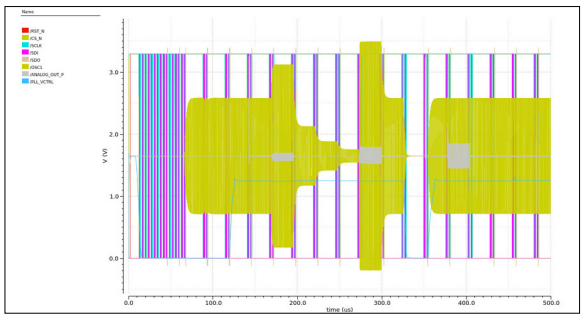
Approach: Based on a literature study, a system design has been defined. The measurement principle relies on a pair of capacitors, one acting as a fixed reference and the other as a variable sensing element. These capacitors are connected in series and excited with differential sinusoidal signals. The sinusoidal signals are generated with an external LC oscillator which is driven by internal cross-coupled transistors. For a potential post-processing, a comparator detects the crossing points of the differential signals and generates digital signals with the same frequency. Another part of this project was the implementation of a phase locked loop (PLL) for four 90° phase-shifted output signals. These digital signals can be used for potential post processing. The first part of the analog chain is a capacitor compensation to eliminate the tolerances of the measurement capacitors. A low noise transimpedance amplifier (TIA) then amplifies the input signal, and a high bandwidth buffer makes the signal available at an output. Both are designed as differential amplifiers. All the mentioned parts were verified with schematic and post-layout simulations in Cadence over multiple corners and Monte Carlo. Special attention for the layout was required due to the challenge of high frequencies. The design is configurable with a serial peripheral interface (SPI) which is implemented in VHDL and tested with Python.

Conclusion: The current design is implemented in a 0.35 um complementary metal oxide semiconductor (CMOS) process. The SPI for configuring the chip is tested and implemented for frequencies of up to 8 MHz. For changeable amplitudes or different external LC-combinations, the oscillator control circuit has a built-in configurable current source with currents of up to 1.8 mA. The PLL works for an output frequency of 50 MHz, resulting in four 90° shifted 12.5 MHz signals. The capacitor compensation is a unique approach and has an integral nonlinearity (INL) of less than 0.04 LSB at seven bit control range. The quantization step is 0.5 fF, ranging from 0 fF to 64 fF. The TIA has a simulated input noise density of approximately 2 nV/(Hz^(1/2)). The output buffer has a gain of two and works as expected. Additional measures were taken to test and verify the design in a future step. For example, the possibility to measure different parts of the designed system on its own. The implemented TIA must undergo a layout redesign due to stability problems, most likely coming from the parasitic capacitances in the current design. In a further step all mentioned blocks need to be put into the prepared padring and connected on the top level of the ASIC. After verification simulations the ASIC must be finalized for fabrication.

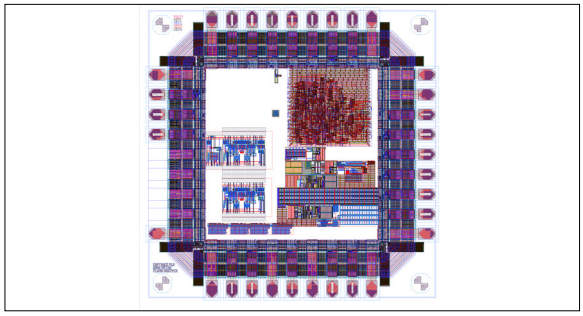
Overview of the implemented design.
Own presentment



Top mixed signal simulation, showing the capability of configuring the ASIC. E.g. configure the oscillation amplitude.
Own presentment



Current version of the top layout. Not Design Rule Check (DRC) clean.
Own presentment



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Subject Area
Electrical Engineering, Sensor, Actuator and Communication Systems